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High-voltage silicon rectifier stacks and their application

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The avalanche rectifier diode is briefly described, together with its ratings. Stack ratings are discussed, particularly with regard to voltage transients and surge currents. Worked examples are given for the selection of a stack for a new installation and to replace a valve rectifier in an existing installation.

INTRODUCTION

Over the past five or six years, the silicon rectifier has been replacing other forms of rectifier in nearly all high-voltage applications. The original high-voltage silicon rectifier stack tended to be cumbersome because it used many low-voltage rectifier diodes with equalising resistors and capacitors. With the introduction of the avalanche rectifier diode, the need for voltage equalising resistors and capacitors is removed and compact stacks can be constructed.

This article considers briefly the avalanche rectifier diode, and provides a guide for its application in high-voltage rectifiers.

THE AVALANCHE RECTIFIER DIODE

An avalanche diode is one which can be operated safely in the reverse avalanche region. With a normal non-avalanche diode, there is a voltage limit above which the diode will break down. This limit is expressed as a working voltage which represents the maximum continuous voltage that can be applied to the diode, and a surge voltage for which a time limit is given. With an avalanche diode, however, exceeding the voltage limit takes the diode into the avalanche region where the breakdown of the diode is determined by the energy it has to dissipate rather than the voltage level. There will, in fact, be an upper voltage limit but generally this is high enough to be disregarded in normal applications.

The advantage of using avalanche diodes in rectifier applications is that the diode will be able to absorb transient energy safely. Often precise information on transients in a particular application is not available, and devices are selected on an assessment of the risk of device failure. Even if generous safety factors are used in the selection of a non-avalanche diode, there is still a risk that an unforeseen very large transient will occur and break down the diode. This risk of breakdown is reduced by using avalanche diodes since the transient energy may be completely absorbed by the diode. It cannot be claimed that the use of avalanche diodes will completely remove the risk of breakdown as the transient energy may be too great for the diode to absorb, but the reliability of the system will be improved.

When diodes are used in series in a high-voltage rectifier stack, there are two main sources of transients. The diodes will encounter transients from the a.c. supply, and also transients will be generated inside the stack itself as the diodes start to conduct after the negative half-cycle of the supply. The diodes will not begin to conduct at the same time, with the result that, depending on the inductance of the circuit, very large reverse recovery transient voltages can be applied to the diodes for very short times. Avalanche diodes are able to absorb these commutation transients, but non-avalanche diodes require equalising resistors and capacitors to ensure that the diode ratings are not exceeded. Thus the cost of a high-voltage stack can be reduced by using avalanche diodes since these ancillary components are not required.

RATINGS OF AVALANCHE DIODES

The four principal ratings of an avalanche diode are: crest working reverse voltage, mean forward current, minimum breakdown (avalanche) voltage, and maximum surge forward current. Apart from the breakdown voltage, these ratings are common to all diodes. The ratings are absolute maximum values, and must not be exceeded.

The crest working reverse voltage V_{RWM} is the maximum peak voltage of a sinewave that can be applied to the diode. It is considered good practice to select a diode with this rating higher than the peak value of the supply on which it is operating, as explained later.

The mean forward current $I_{F(AV)}$ is the maximum mean current averaged over 20ms that can be taken from the diode operating in a specified ambient temperature.

The minimum breakdown (avalanche) voltage $V_{(BR)R}$min is the reverse voltage above which the diode operates in the avalanche region. Operation in this region depends on the energy to be dissipated by the diode. If the energy levels of transients for a particular application are not known, it is necessary to select a diode with a minimum breakdown voltage greater than the expected voltage level of the transients, or to limit the voltage of transients to below the breakdown voltage of the diode.

The maximum surge forward current I_{FSM} is the maximum peak value of a 10ms half-sinewave current that can be taken from the diode. This rating is used for fault conditions. It represents the maximum current that should be taken from the diode before a fuse or circuit breaker isolates the stack.

When avalanche diodes are connected in series to form a stack, the crest working voltage and breakdown voltage of the stack are the sum of the ratings of the individual diodes. Thus for an OSS9110-3 stack containing three BYX39-1000R avalanche diodes, the stack has a V_{RWM} rating of 3kV (3×1kV for the individual diodes), and a $V_{(BR)R}$min rating of 3·75kV (3×1·25kV for the individual diodes). The value of the stack I_{FSM} rating is the same as that of the individual diodes, while the $I_{F(AV)}$ rating depends on the method of cooling the stack.

Curves of the mean current rating plotted against ambient temperature for the Mullard range of high-voltage rectifier stacks are shown in Fig. 1. These curves are for natural convection cooling; higher currents can be obtained with forced-air cooling or oil cooling.

The surge current ratings of the range are shown in Fig. 2 where the maximum r.m.s. surge current is plotted against surge duration. These curves are used to design protective circuits for most applications, but sometimes it is necessary to use a 'crowbar' circuit to remove the d.c. supply from the load very rapidly. In applications where this is likely to occur regularly, say two or three times an hour, it is advisable to use a surge current rating of two-thirds the value given in Fig. 2.

CONSTRUCTION OF STACK

High-voltage stacks are constructed from a series of interlocking 'vertebrae' on which the avalanche diodes and heatsinks are mounted. The diodes are bolted to preformed heatsinks made from black anodised aluminium. Three heatsinks are fitted onto a vertebra, and up to ten vertebrae can be connected together to form a stack of 30 diodes and heatsinks. The vertebrae are moulded from impregnated glass fibre to give the properties required for a high-voltage insulator. Interconnections between the individual diodes are made by means of the flexible cathode leads. Three configurations are possible for the stacks: series connection, push-pull (inverse-series connection with centre tap), and doubler (series connection with centre tap). The three configurations with the corresponding type number prefix are shown in Fig. 3.

Three methods of mounting are possible with the stacks. These are: ¼in U.N.F. stud, valve base, and goliath edison screw cap. A typical stack containing 12 diodes

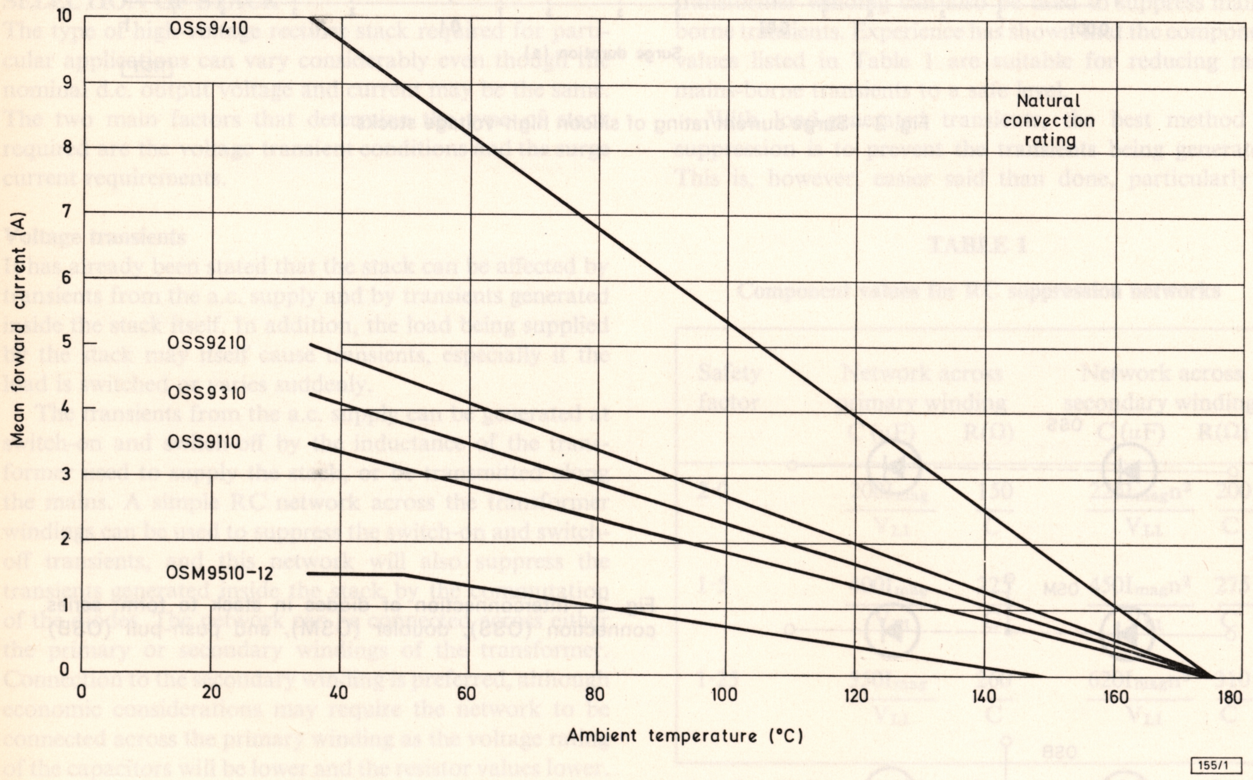

Fig. 1—Mean current rating of silicon high-voltage stacks

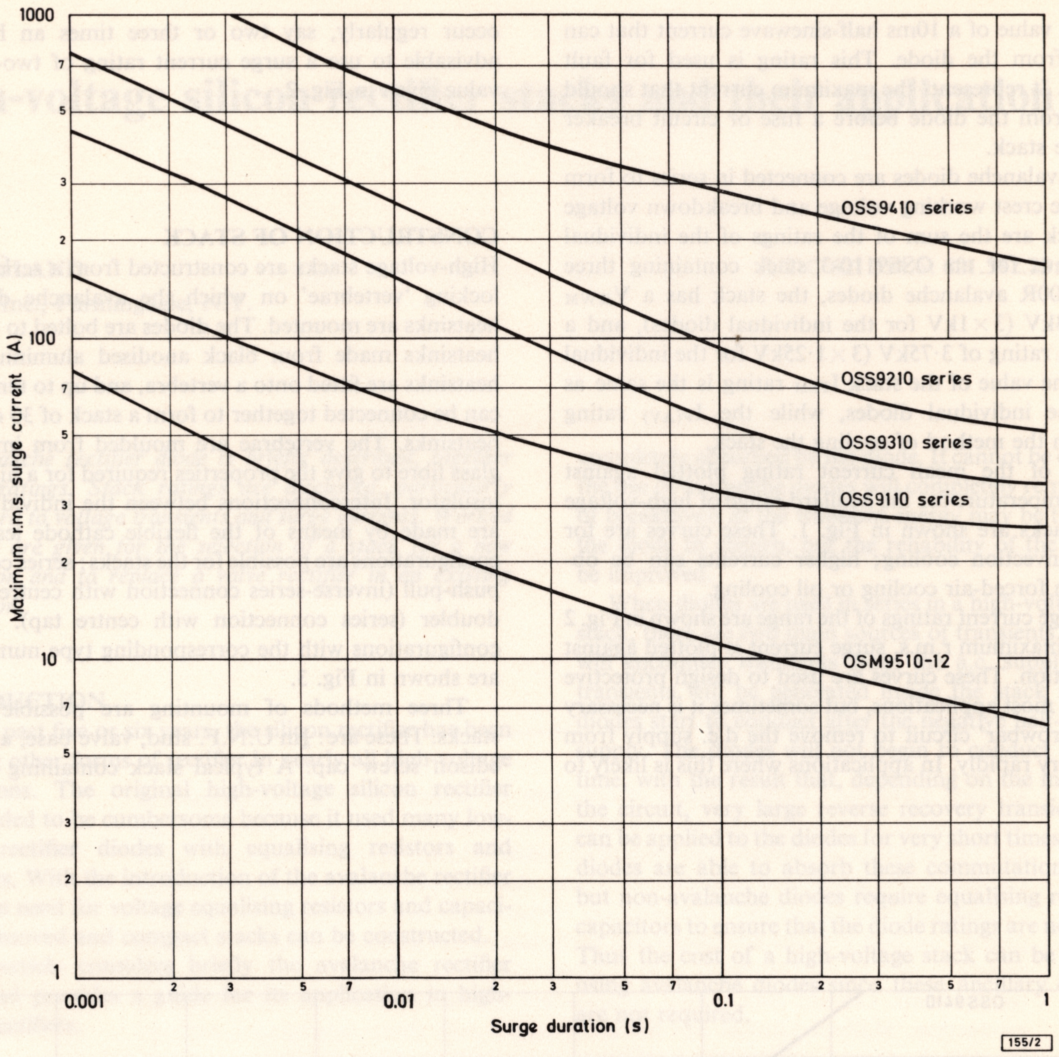

Fig. 2—Surge current rating of silicon high-voltage stacks

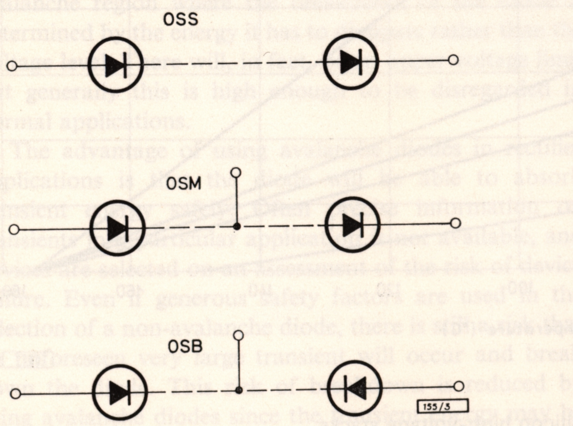

Fig. 3—Interconnection of diodes in stack to form: series connection (OSS), doubler (OSM), and push-pull (OSB)

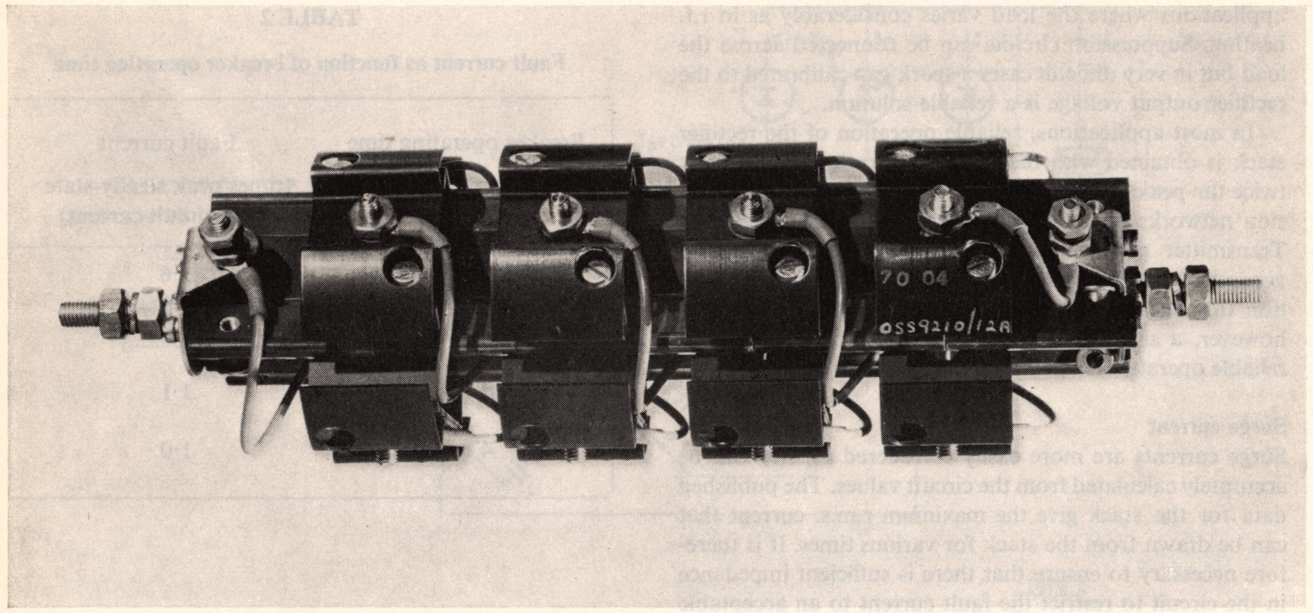

Fig. 4—High-voltage silicon stack containing 12 avalanche rectifier diodes and fitted with stud mounting

with stud mounting is shown in the photograph of Fig. 4.

A different method of construction is used for the OSM9510-12 stack. This stack, which uses wire-ended diodes, is encapsulated as a rectangular block fitted with mounting lugs.

SELECTION OF STACK

The type of high-voltage rectifier stack required for particular applications can vary considerably even though the nominal d.c. output voltage and current may be the same. The two main factors that determine the type of stack required are the voltage transient conditions and the surge current requirements.

Voltage transients

It has already been stated that the stack can be affected by transients from the a.c. supply and by transients generated inside the stack itself. In addition, the load being supplied by the stack may itself cause transients, especially if the load is switched or varies suddenly.

The transients from the a.c. supply can be generated at switch-on and switch-off by the inductance of the transformer used to supply the stack, or be transmitted along the mains. A simple RC network across the transformer windings can be used to suppress the switch-on and switch-off transients, and this network will also suppress the transients generated inside the stack by the commutation of the diodes. The network can be connected across either the primary or secondary windings of the transformer. Connection to the secondary winding is preferred, although economic considerations may require the network to be connected across the primary winding as the voltage rating of the capacitors will be lower and the resistor values lower.

A typical circuit of a delta-star transformer supplying a high-voltage rectifier is shown in Fig. 5. The RC suppression networks are shown connected across the secondary windings. The component values depend on the magnetising primary current of the transformer, the primary voltage, and the voltage ratio of the transformer. A safety factor can be incorporated, and values of suppression components for three safety factors are listed in Table 1.

The RC network together with the inductance of the transformer winding can also be used to suppress mains-borne transients. Experience has shown that the component values listed in Table 1 are suitable for reducing most mains-borne transients to a safe level.

With load-generated transients, the best method of suppression is to prevent the transients being generated. This is, however, easier said than done, particularly in

TABLE 1

Component values for RC suppression networks

Safety factor	Network across primary winding C (μF)	Network across primary winding R(Ω)	Network across secondary winding C (μF)	Network across secondary winding R(Ω)
2·0	$\frac{200I_{mag}}{V_{L1}}$	$\frac{150}{C}$	$\frac{225I_{mag}n^2}{V_{L1}}$	$\frac{200}{C}$
1·5	$\frac{400I_{mag}}{V_{L1}}$	$\frac{225}{C}$	$\frac{450I_{mag}n^2}{V_{L1}}$	$\frac{275}{C}$
1·25	$\frac{550I_{mag}}{V_{L1}}$	$\frac{260}{C}$	$\frac{620I_{mag}n^2}{V_{L1}}$	$\frac{310}{C}$

where I_{mag} is the magnetising primary current of the transformer, V_{L1} the primary line-to-line voltage, and n the transformer ratio ($n = V_{L1}/V_{L2}$ where V_{L2} is the secondary line-to-line voltage).

applications where the load varies considerably as in r.f. heating. Suppression circuits can be connected across the load but in very difficult cases a spark gap calibrated to the rectifier output voltage is a reliable solution.

In most applications, reliable operation of the rectifier stack is obtained with the $V_{(BR)R}$min rating of the stack twice the peak voltage of the a.c. supply when RC suppression networks are used across the transformer windings. Transmitter power supplies are normally less likely to generate transients, and so with the stacks for this application this safety factor can be lowered. With r.f. heating, however, a safety factor of at least two is necessary for reliable operation.

Surge current

Surge currents are more easily considered as they can be accurately calculated from the circuit values. The published data for the stack give the maximum r.m.s. current that can be drawn from the stack for various times. It is therefore necessary to ensure that there is sufficient impedance in the circuit to restrict the fault current to an acceptable level until the circuit breaker or fuse isolates the stack from the supply. This can often be achieved by specifying a transformer with the necessary percentage impedance.

When a fault occurs, the current will rise to a peak and then decay towards the peak steady-state short-circuit current. If a circuit breaker is used to isolate the stack from the supply, a certain time will elapse before it operates. The surge current rating I_{FSM} of the stack must be greater than the value of fault current at the time the circuit breaker operates. In Table 2 the operating time of the circuit breaker is expressed in terms of cycles of the 50Hz supply. The corresponding values of fault current are listed as multiplying factors for the steady-state short-circuit current. This current can be calculated for the particular application, and from this the required surge current rating of the stack determined.

TABLE 2

Fault current as function of breaker operating time

Breaker operating time (number of cycles)	Fault current (times peak steady-state short-circuit current)
1	1·6
2	1·3
3	1·1
4 or more	1·0

In some applications, fuses in the primary circuit of the transformer may be used for fault protection. If high-speed fuses are used, it may be possible to use a smaller stack than would otherwise be necessary. For full protection, the I^2t value of the fuse referred to the secondary winding of the transformer must be less than the I^2t value of the stack. Thus:

$$I^2t_{\text{ fuse}} \times n^2 < I^2t_{\text{ stack}},$$

where n is the ratio of the primary to secondary line-to-line voltages. The I^2t rating of the stack is the same as that of the individual diodes.

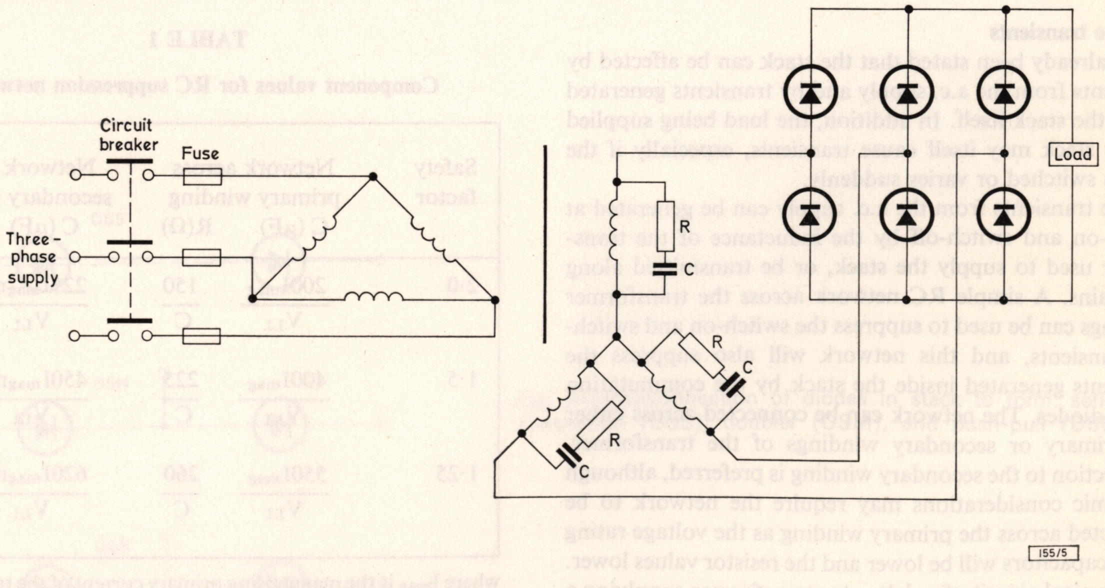

Fig. 5—Delta-star transformer supplying rectifier in typical high-voltage application

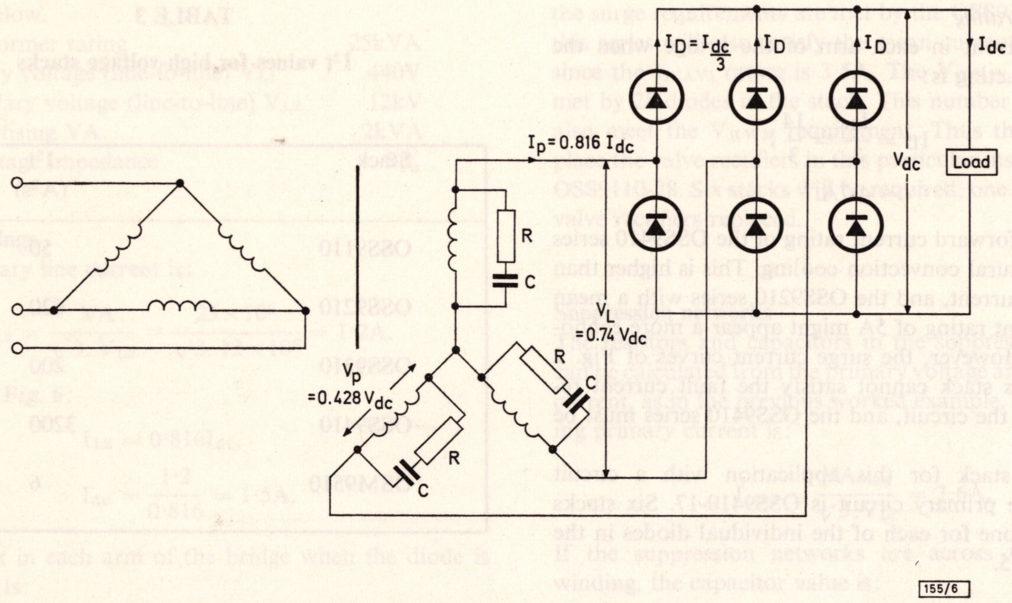

Fig. 6—Relationships between a.c. and d.c. voltages and currents in circuit of Fig. 5. The d.c. current and voltage are taken as unity

Example

As an example of the calculations leading to the selection of a stack, the circuit shown in Fig. 5 will be supposed to deliver 14A at 10kV into the load. The magnetising primary current of the transformer is 6A.

Voltage ratings

The relationships between the a.c. and d.c. voltages and currents are shown in Fig. 6. For a d.c. output voltage from the stack of 10kV, the r.m.s. line-to-line voltage applied to the stack is:

$$V_{L2} = 0{\cdot}74V_{dc} = 7{\cdot}4\text{kV}.$$

Thus the peak voltage applied to each diode in the stack is:

$$\sqrt{2}.V_{L2} = 1{\cdot}41 \times 7{\cdot}4 = 10{\cdot}5\text{kV},$$

and the V_{RWM} rating of the stack must satisfy this requirement.

Allowing a safety factor of 2 between the peak voltage across the diode and the minimum breakdown voltage, the $V_{(BR)R}$min rating of the stack is:

$$V_{(BR)R}\text{min} = 2 \times 10{\cdot}5 = 21\text{kV}.$$

This requirement of 21kV can be met by 17 diodes with an individual $V_{(BR)R}$min rating of 1·25kV connected in series to give:

$$\text{stack } V_{(BR)R}\text{min} = 17 \times 1{\cdot}25 = 21{\cdot}25\text{kV}.$$

This stack will also meet the V_{RWM} requirement of 10·5kV since the individual V_{RWM} rating of the diodes is 1kV, giving a stack V_{RWM} rating of 17kV.

Surge current rating

The transformer r.m.s. secondary phase voltage is:

$$V_{P2} = 0{\cdot}428V_{dc},$$

and the secondary r.m.s. phase current is:

$$I_{P2} = 0{\cdot}816I_{dc}.$$

Thus the transformer secondary VA rating is:

$$3V_{P2}I_{P2} = 3 \times 0{\cdot}428 \times 0{\cdot}816V_{dc}I_{dc}, \\ = 146\text{kVA}.$$

The short-circuit VA rating is:

$$VA_{sc} = \frac{VA}{Z_{pc}},$$

where Z_{pc} is the percentage impedance of the transformer, which for high-voltage transformers is generally 5%. The peak steady-state short-circuit current is given by:

$$I_{sc(M)} = \frac{\sqrt{2}.\ VA_{sc}}{\sqrt{3}.\ V_{L2}} = \frac{\sqrt{2}.\ (146/0{\cdot}05)}{\sqrt{3}.\ 7{\cdot}4}, \\ = 321\text{A}.$$

If a circuit breaker is used and the breaker operates within two cycles of the supply after the fault occurs, the fault current will be (from Table 2):

$$I_{fault} = 1{\cdot}3 \times I_{sc(M)} = 418\text{A}.$$

The surge current rating of the stack at two cycles (40ms) must be greater than this value. The surge currents plotted in Fig. 2 are given as r.m.s. values. The fault current calculated above is a peak value, and converting this to an r.m.s. value gives:

$$I_{fault\ (r.m.s.)} = I_{fault} \times \frac{1}{\sqrt{2}}, \\ = 295\text{A}.$$

From the curves in Fig. 2 it can be seen that the OSS9410 series will satisfy this requirement.

Mean current rating

The mean current in each arm of the bridge when the diode is conducting is:

$$I_D = \frac{I_{dc}}{3} = \frac{14}{3},$$
$$= 4\cdot7\text{A}.$$

The mean forward current rating of the OSS9410 series is 10A for natural convection cooling. This is higher than the required current, and the OSS9210 series with a mean forward current rating of 5A might appear a more economical stack. However, the surge current curves of Fig. 2 show that this stack cannot satisfy the fault current requirements of the circuit, and the OSS9410 series must be used.

Thus the stack for this application with a circuit breaker in the primary circuit is OSS9410-17. Six stacks are required, one for each of the individual diodes in the circuit of Fig. 5.

Protection by fuses

Fuses in the primary circuit can be used for protection in place of the circuit breaker. If the transformer is operating from the 440V three-phase mains, the step-up ratio is:

$$\frac{V_{L2}}{V_{L1}} = \frac{7\cdot4\times10^3}{440} = \frac{1}{n}.$$

Since the secondary phase current is 0·816 × 14A, the primary phase current is:

$$I_{P1} = 0\cdot816\times14\times\frac{1}{n},$$
$$= 192\text{A}.$$

A 200A fuse would be used to protect this circuit, with a typical I^2t value of 20 000. Transferring this to the secondary winding of the transformer:

$$I^2{}_{\text{fuse}} = 20\,000\left(\frac{440}{7\cdot4\times10^3}\right)^2$$
$$=71\text{A}^2\text{s}.$$

The I^2t value of the stack must be greater than this value.

The I^2t values for the range of stacks are listed in Table 3. From this it can be seen that the OSS9310 series with an I^2t of $200\text{A}^2\text{s}$ is the nearest to satisfy this requirement. Since the mean forward current rating of the OSS9310 series is 4·0A, it will not meet the mean current requirement and so the OSS9210 series with an I^2t value of $620\text{A}^2\text{s}$ and a mean forward current rating of 5·0A must be used. Compared with the 10A rating of the OSS9410 series, the use of an OSS9210 stack with fuses in the primary circuit represents a more economical solution for this application.

TABLE 3

I^2t values for high-voltage stacks

Stack	I^2t (A^2s)
OSS9110	50
OSS9210	620
OSS9310	200
OSS9410	3200
OSM9510	6

Suppression networks

The values of the components in the RC suppression networks for use with both fuses and a circuit breaker are derived from the expressions in Table 1.

The magnetising current is 6A, and a safety factor of 2 is required. The capacitor across the secondary winding is, from the expression in Table 1:

$$C = 225\,\frac{I_{mag}n^2}{V_{L1}} = \frac{225\times6\times(440/7400)^2}{440},$$
$$= 0\cdot01\mu\text{F}.$$

The corresponding resistance is:

$$R = \frac{200}{C} = \frac{200}{0\cdot01},$$
$$= 20\text{k}\Omega.$$

The r.m.s. voltage rating of the capacitor is at least 7·4kV, and the power rating of the resistance is approximately 11W. If the suppression networks are connected across the primary windings, the component values are:

$$C = 2\cdot7\mu\text{F, voltage rating 440V,}$$
$$R = 55\Omega\text{, power rating 8W.}$$

SELECTION OF STACK TO REPLACE VALVE RECTIFIER

Silicon rectifiers can be used to replace valve gasfilled rectifiers in existing installations. For this purpose, the range of silicon stacks can be provided with standard valve bases for mounting. It is not possible, however, to provide a simple replacement list since the characteristics of valve and semiconductor rectifiers are different. Instead, it is necessary to consider each application individually. As a guide to the procedure involved, a worked example will be given.

It can be assumed that since the transformer supplying the valve rectifiers gave the required d.c. voltage and current, the replacement by a silicon rectifier will not materially affect the d.c. output. It is only necessary therefore to ensure that the silicon stack is suitable for the surge current conditions. The transformer characteristics will be known, and typical figures for a circuit of the type shown in Fig. 5 are listed below.

Transformer rating	25kVA
Primary voltage (line-to-line) V_{L1}	440V
Secondary voltage (line-to-line) V_{L2}	12kV
Magnetising VA	2kVA
Percentage impedance	5%

Current ratings

The secondary line current is:

$$I_{L2} = \frac{VA}{\sqrt{3}.\,V_{L2}} = \frac{25\times10^3}{\sqrt{3}.\,12\times10^3} = 1\cdot2\text{A}.$$

Since from Fig. 6:

$$I_{L2} = 0\cdot816 I_{dc},$$
$$I_{dc} = \frac{1\cdot2}{0\cdot816} = 1\cdot5\text{A}.$$

The current in each arm of the bridge when the diode is conducting is:

$$I_D = \frac{I_{dc}}{3},$$

therefore the mean forward current rating of the stack is:

$$I_{F(AV)} = \frac{1\cdot5}{3} = 0\cdot5\text{A}.$$

The peak steady-state short-circuit current is given by:

$$I_{sc(M)} = \frac{\sqrt{2}.\,VA_{sc}}{\sqrt{3}.\,V_{L2}} = \frac{\sqrt{2}.\,(25\times10^3/0\cdot05)}{\sqrt{3}.\,12\times10^3}.$$
$$= 34\text{A}.$$

If the circuit breaker is expected to isolate the stack within the first cycle of the supply after the occurrence of the fault, the peak fault current is:

$$I_{\text{fault}} = 1\cdot6\times I_{sc(M)} = 54\text{A}.$$

Converting this peak value to an r.m.s. value gives the surge rating of the required stack as:

$$I_{\text{fault(r.m.s.)}} = 38\text{A}.$$

Voltage rating

The crest working voltage of the stack must be greater than the peak secondary line voltage; that is:

$$V_{RWM}\text{min} = \sqrt{2}.12 = 17\text{kV}.$$

Allowing a safety factor of 2 gives:

$$V_{(BR)R}\text{min} = 2\times17 = 34\text{kV}.$$

Required ratings

The ratings of the replacement stack are therefore:

r.m.s. surge current rating $> 38\text{A}$ at 20ms duration,
$I_{F(AV)} > 0\cdot5\text{A},$
$V_{(BR)R}\text{min} > 34\text{kV},$
$V_{RWM} > 17\text{kV}.$

From the surge current curves in Fig. 2 it can be seen that the surge requirements are met by the OSS9110 series, and this series will also satisfy the mean current requirements since the $I_{F(AV)}$ rating is 3·5A. The $V_{(BR)R}$ rating will be met by 28 diodes in the stack. This number of diodes will also meet the V_{RWM} requirement. Thus the stack to replace the valve rectifiers in this particular installation is the OSS9110-28. Six stacks will be required, one for each of the valve rectifiers replaced.

Suppression networks

The resistors and capacitors in the suppression networks can be calculated from the primary voltage and magnetising current, as in the previous worked example. The magnetising primary current is:

$$I_{mag} = \frac{VA_{mag}}{\sqrt{3}.V_{L1}} = 2\cdot6\text{A}.$$

If the suppression networks are across the secondary winding, the capacitor value is:

$$C = \frac{225\times2\cdot6\,(440/12\,000)^2}{440},$$
$$= 0\cdot0018\mu\text{F};$$

and the resistance value is:

$$R = \frac{200}{C} = 111\text{k}\Omega.$$

The r.m.s. voltage rating for the capacitor is 12kV, and the power rating for the resistance is 5W.

If the suppression networks are connected across the primary windings of the transformer, the component values are:

$$C = 1\cdot2\mu\text{F, voltage rating 440V,}$$
$$R = 126\Omega\text{, power rating 3·5W.}$$

APPLICATIONS

The two main applications for high-voltage rectifier stacks have already been mentioned in discussing the selection of stacks. The applications are in the power supplies for radio and television transmitters, and for r.f. heating equipment. Different requirements are imposed on the stacks for these applications, and these requirements affect the ratings by which the stack is selected for a particular application. Provided these ratings are properly chosen, the silicon rectifier stack will give satisfactory service.

Experience with these stacks has shown that not only will they operate satisfactorily in applications for which mercury-vapour rectifiers have previously been used, but they can also offer advantages over valve rectifiers. As the stack requires no heater, there is no need for a high-voltage insulated heater transformer. There is no warm-up time so the installation is immediately available for use, and the stack can operate satisfactorily in an ambient temperature higher than that permissible for valve rectifiers.

Data on the range of high-voltage rectifier stacks are contained in the Mullard Technical Handbook, Book 1, Part 4.

Channel electron multipliers

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UDC 621.383.81

Channel electron multipliers detect and amplify input stimulations of electrons, ions, short wavelength ultraviolet radiation and both soft and diagnostic quality X-radiation. They have a typical gain of $1{\cdot}5\times10^8$ at 3·0kV, and can detect single electrons. This article discusses principles of construction and operation, and gives details of various applications.

INTRODUCTION

Channel electron multipliers were originally developed for the direct study of the various radiation belts surrounding the Earth. The multipliers respond to electrons, ions, short wavelength ultraviolet radiation and both soft and diagnostic-quality X-radiation. Because they are small and rugged, have a high electron gain and require only minute power, they are well suited for rocket and satellite payloads. The channel electron multiplier also has a number of laboratory applications in the fields of mass and ultraviolet spectroscopy.

Some of the properties and features of the channel electron multiplier are as follows:

windowless input,
high electron gain,
low background count rate,
low power consumption,
compactness, ruggedness and lightness, and
simplicity of use.

The channel electron multipliers described here are available in a range of shapes including variants with flared input apertures. The output ends of the multipliers may be open or closed, depending on whether d.c. or pulse-counting operation is intended.

This article contains information on currently available channel electron multipliers, defines their principal characteristics, and stipulates a number of limiting operating conditions.

PRINCIPLES OF CONSTRUCTION AND OPERATION

A channel electron multiplier is a small curved glass tube, the inside wall of which is coated with a resistive material. If a potential is applied between the ends of the tube, the resistive surface becomes a continuous dynode, electrically analogous to the separate dynodes of a conventional photomultiplier together with the resistive chain used to establish the separate dynode potentials.

The channel electron multiplier operates in vacuum. For space research, the environmental vacuum is sufficient but in the laboratory, the multiplier must be used in a vacuum chamber.

An electron entering the negative potential end of the channel multiplier generates secondary electrons on collision with the wall of the tube. These are accelerated along the tube until they strike the wall again, where they generate further secondary electrons. This avalanching process produces a large number of electrons at the positive end of the tube. This is illustrated in Fig. 1. These electrons appear as an output pulse that may contain up to 10^8 electrons, whose amplitude depends on the values of resistance and capacitance in the anode circuit of the multiplier. The gain G, defined as the magnitude of the output pulse for one single input event, is an exponential and very steep function of voltage for values below 10^7 (Fig. 2). Above 10^7 saturation effects are observed which will be discussed later.

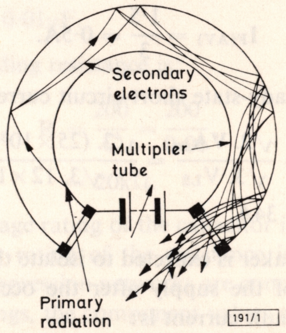

Fig. 1—Electron multiplication

The multiplier will respond to ions, particles, X-rays and other radiation. The detection efficiency varies for different forms of excitation, but any particle or quantum capable of exciting an electron from the dynode surface has a finite probability of detection.

Since the resistive layer is continuous, many electron paths are possible, and the number of stages of multiplication is thus indeterminate. The electron trajectories are scaled in proportion to the dimensions of the channel for a given applied voltage. Thus if the length-to-diameter ratio is preserved, the same multiplication processes go on, and the same gain is achieved, irrespective of the absolute length of the channel. In practice it is necessary for the length to diameter ratio to exceed about 30:1. Channels are usually curved, and the gain is then less critically dependent on the length-to-diameter ratio. The ratios used are between 50:1 and 100:1.

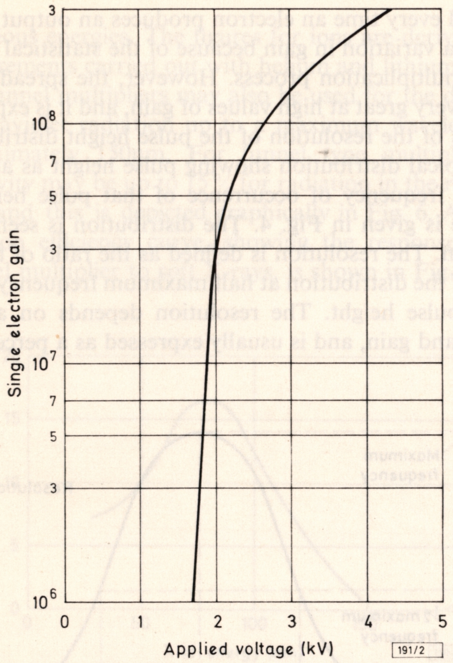

Fig. 2—Typical variation of gain with applied voltage

Ionic feedback

The tube forming the channel multiplier is curved because the gain of a straight tube would be sensitive to changes in vacuum pressure. When the first cloud of electrons nears the output end of the mutliplier, it is sufficiently dense to ionise a considerable number of the residual gas atoms in the tube. These positive ions drift under the influence of the applied field towards the more negative potential at the input end of the channel.

If the channel is straight, the ions may acquire considerable energy before they collide with the wall of the tube. Consequently they may release electrons from the wall which will initiate a further multiplication through the tube, resulting in a spurious pulse. This process is repeated and thus a sequence of after pulses may be observed, lasting approximately one microsecond until the channel capacity is exhausted.

In a curved tube, the ions strike the wall of the tube before they have acquired sufficient energy to release secondary electrons. Electron multiplication is unaffected, since electrons need only to acquire an energy of about 50eV to release secondaries from the wall. The output of the curved multiplier is therefore virtually independent of ambient pressure, provided the latter does not exceed 6×10^{-2} Nm^{-2}. Above this pressure, spurious pulses occur, and effects similar to those seen with straight channels are observed.

Saturation effects

Another significant aspect of the behaviour of a channel multiplier is the saturation effect caused by space-charge limitation. When the total amount of charge in the electron cloud in a channel multiplier reaches about 3×10^8 electrons, the gain cannot increase further. The space charge repels the emitted secondary electrons so that they strike the wall before acquiring sufficient energy from the field to make useful multiplying collisions. The space-charge limit is unaffected by the channel diameter. Increasing the applied voltage increases the amplitude of those pulses which would not otherwise have reached 3×10^8 electrons, but as the maximum charge output cannot exceed this level, the amplitude of all the pulses tends to the same value. When the multiplier is operated in this saturated mode, it is analogous to a Geiger counter, producing a pulse of given amplitude irrespective of the manner of its excitation. It is unable in this condition to give information about the energy of the input stimulus or about the number of particles if they enter the input simultaneously.

When the multiplier is not operated in its saturated mode, that is, when the gain is less than 10^7, there is some proportionality between the input and output. However, there is a spread of pulse amplitudes because of the many possible electron paths through the multiplier. In this condition the pulse amplitude distribution is found to be approximately exponential, with smaller pulses being more probable than larger ones by an amount dependent on their amplitude.

As the channel multiplier curvature eliminates the possibility of after pulses it is possible for the channel to produce a second pulse immediately after the passage of the first. If the mean pulse repetition rate is high, the field inside the channel is distorted. A state of dynamic equilibrium is then achieved, where the mean gain is reduced so that the average rate of flow of charge in the output pulses remains less than the charge that can be extracted from the resistive layer.

CHARACTERISTICS

Resistance

The resistance of a channel electron multiplier depends on the size of the channel and the material used for the resistive layer. The multipliers described in this article have an internal surface film of metallic lead. Their nominal resistance lies in the range 10^9 to $10^{10}\Omega$ at 20°C and they have a negative temperature coefficient. For example, if the multiplier resistance at 20°C is $R\Omega$ then at 40°C its value will be $0{\cdot}6R\Omega$. At -30°C the resistance will increase to $1{\cdot}7R\Omega$.

Background pulse count rate

The background or spontaneous pulse count rate is the number of output pulses produced per second above a specified amplitude when the input end of the multiplier is closed. The count is made at a specified multiplier voltage and equivalent threshold. Thus only pulses of greater amplitude than the equivalent or amplifier threshold pass into the amplifier.

There is no appreciable variation of background count rate when either the applied voltage or the ambient temperature is changed.

Starting voltage

As the voltage applied to the channel is increased, the gain rises and the output pulses become larger. The pulses are not all the same size but as the gain increases, more of them exceed the equivalent threshold. This process continues until the pulses are above the threshold. If the observed count rate is plotted against voltage, as indicated in Fig. 3, then the curve will show a steeply rising portion followed by a plateau.

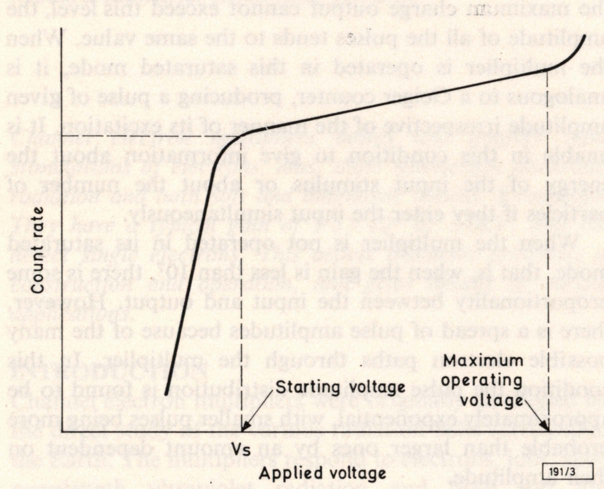

Fig. 3—Definition of starting voltage

The starting voltage V_s is selected so that 90% of the output pulses from single electron inputs exceed a specified threshold.

The starting voltage is measured with an input source adjusted to give a fixed count rate at a high applied voltage.

Gain

The output pulse corresponding to one input electron will consist of G electrons. The corresponding charge in the output pulse will thus be $G\times1{\cdot}6\times10^{-19}$ coulombs, where $1{\cdot}6\times10^{-19}$ coulombs is the electronic charge. If a pulse amplifier is connected to the output of the multiplier the charge in the pulse will raise the potential across the input capacitance of this amplifier. The voltage change produced is referred to as the pulse height (usually in millivolts).

The gain is dependent on the voltage applied to the multiplier and is affected by the input count rate.

Because of the finite resistance of the channel multiplier, there is a recovery period after the passage of a pulse while the potential distribution is restored to its original form. This means that, above a certain level, as the electron input rate is increased, the mean output pulse level decreases. Therefore the gain is constant up to a count rate of 1000 pulses per second and then falls to a third of its value at 10^4 pulses per second. Above this the gain falls by approximately 10dB per factor of ten increase in count rate. In practice, the count rate capability of the multiplier may be increased by lowering the external measuring threshold. Thus, high count rates may be achieved at the expense of reduced gain.

Resolution

The nominal gain of a channel multiplier will not be achieved every time an electron produces an output pulse: there is a variation in gain because of the statistical nature of the multiplication process. However, the spread is not usually very great at high values of gain, and it is expressed in terms of the resolution of the pulse height distribution.

A typical distribution showing pulse height as abscissa and the frequency of occurrence of that pulse height as ordinate is given in Fig. 4. The distribution is seen to be Gaussian. The resolution is defined as the ratio of the full width of the distribution at half maximum frequency to the modal pulse height. The resolution depends on applied voltage and gain, and is usually expressed as a percentage.

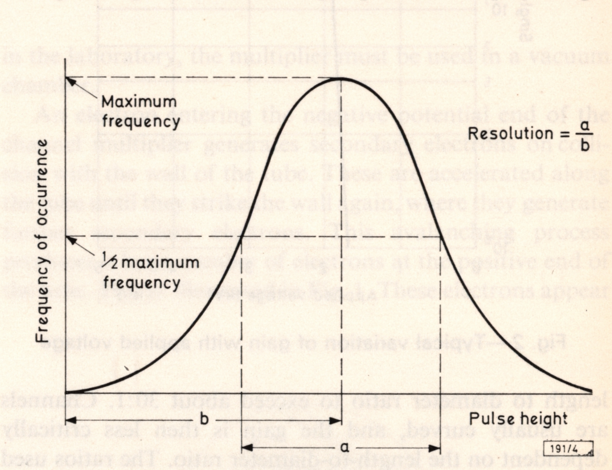

Fig. 4—Definition of resolution of pulse distribution height

Input aperture

Larger input apertures can be achieved by producing multipliers with flared ends. Because the response of a channel multiplier depends on the angle of incidence of the input flux, it is not practicable to quote dimensions of effective apertures which are valid in all situations. The effective aperture of a multiplier is not necessarily the same as the geometrical aperture, but may be smaller.

Sensitivity

The detection efficiency of the multiplier is defined as the percentage of input particles or quanta producing detectable pulses at the output.

Fig. 5 shows the typical detection efficiency of the channel multiplier for electrons, protons and positive ions of various energies. The figures for ions are derived from measurements carried out with helium and lithium ions.

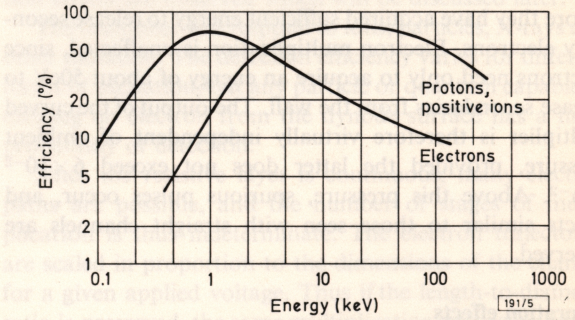

Fig. 5—Typical detection efficiency for electrons, protons and positive ions

Channel multipliers may also be used for the detection of ultraviolet radiation up to a maximum wavelength of approximately 150nm. For funnel type multipliers the sensitivity may be up to 15% for radiation in the region of 70nm and this is depicted graphically in Fig. 6. A typical detection efficiency curve, showing the response of the channel multiplier to soft X-rays, is shown in Fig. 7.

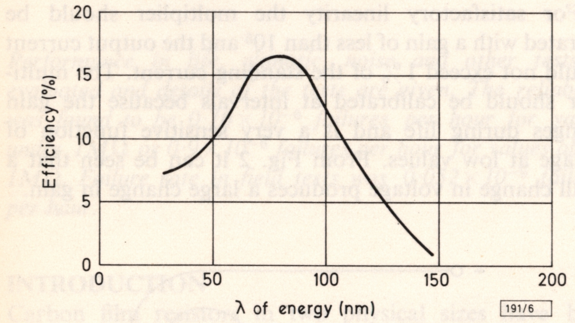

Fig. 6—Detection efficiency for ultraviolet radiation

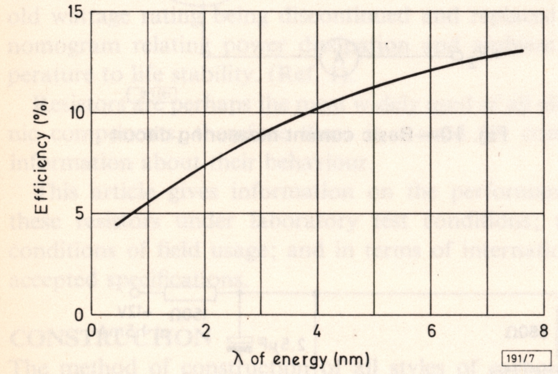

Fig. 7—Detection efficiency for soft X-radiation

Response time

When a single input event is detected by the channel multiplier an output pulse is produced having a duration of about 12 nanoseconds. The duration is defined as the full pulse width at 50% of the peak height. The pulse rise time is approximately 5 nanoseconds.

Temperature

During operation the temperature of the channel multiplier must not exceed 70°C. Standard multipliers may be vacuum baked up to a temperature of 120°C but voltage must not be applied during this operation. By employing different manufacturing techniques, multipliers able to withstand vacuum bake-out temperatures up to 400°C can be produced. A high temperature bake-out will produce a slight loss of gain. For example, a 16-hour bake at 400°C will result in a drop in gain to half its original value.

It should be remembered that if the ambient temperature is reduced there is an increase in the multiplier resistance. This will limit the maximum count rate capability as the resistive layer is unable to supply sufficient charge.

Environment

The channel multiplier operates most efficiently at vacuum pressures between $6\times10^{-2}N_m^{-2}$ and $1\times10^{-6}N_m^{-2}$. Above $6\times10^{-2}N_m^{-2}$ after-pulsing can occur as discussed previously, and at pressures lower than $1\times10^{-6}N_m^{-2}$ it is possible that there will be a decrease in gain after prolonged use. This fatiguing effect is usually defined as the loss of gain after a certain number of accumulated output pulses. Typical multipliers show a fairly constant gain up to a total of 10^{10} accumulated counts, after which a reduction of gain between three and ten times may be observed as the total of accumulated counts rises to 10^{11}. To obtain optimum efficiency normal vacuum precautions should be observed. In particular gross contamination with hydrocarbon vapours should be avoided as this will cause rapid loss of gain.

Channel multipliers can also be affected by external fields. Magnetic fields up to 0·02 tesla parallel to the plane of the helix have little effect on the performance, but above this level and with fields perpendicular to the helix plane, magnetic screening should be employed. Care should be taken to ensure that the multiplier is adequately screened from particles other than those required to be detected. Extraneous radiation can stimulate multiplication processes that will give rise to an increase in the background pulse count rate.

APPLICATION NOTES

Pulse counting mode

The narrow pulse height distribution and high electron gain characteristics of the channel multiplier make it very suitable for pulse counting applications. The operating voltage should be chosen so that all of the multiplier output pulses are above the discriminator threshold—that is, they should be above the equivalent threshold. This can be achieved by setting the operating voltage above the starting voltage.

If the equivalent threshold of the measuring system is higher than 2×10^7 electrons then the starting voltage must be measured for the particular threshold used. This can be determined by plotting the curve of count rate against applied voltage at a constant input rate. A suitable input source of low energy β-particles is tritium, which is available absorbed on a layer of titanium, plated onto copper. The source should be electrically connected to the input of the multiplier.

If the equivalent threshold of the measuring system is lower than 2×10^7 electrons, a lower applied voltage may be used than the quoted starting voltage, but the results must be interpreted carefully. As the multiplier gain is reduced, the pulse height distribution broadens and becomes exponential. Under these conditions there is a possibility that some pulses will be lost below the threshold. To minimise this effect, and to ensure that changes in gain do not influence the output count rate, it is advisable to set the equivalent threshold well below the modal pulse amplitude.

For most applications some form of intermediate amplifier is required between the channel multiplier and its measuring equipment. Two systems are shown in Fig. 8.

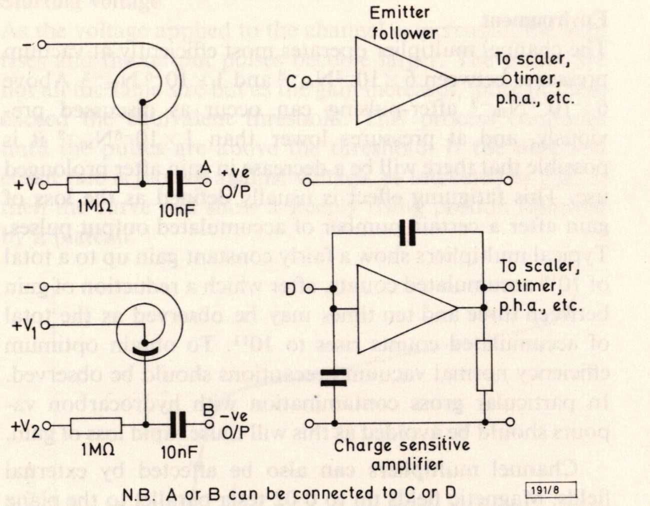
Emitter follower
To scaler, timer, p.h.a., etc.
C
−
+V
1MΩ
10nF
A
+ve O/P
To scaler, timer, p.h.a., etc.
D
−
+V1
+V2
1MΩ
10nF
B
−ve O/P
Charge sensitive amplifier
N.B. A or B can be connected to C or D
191/8

Fig. 8—Some channel multiplier connecting arrangements

The emitter follower offers a simple solution, but it has the disadvantage that it must be placed as close as possible to the channel multiplier output in order to preserve the pulse information. In most cases it is necessary to place it inside the vacuum system.

The charge sensitive amplifier can be used effectively here because its output voltage is almost independent of its input capacitance loading, consequently a long cable can be used to connect it to the output of the multiplier. A simple circuit is shown in Fig. 9. The noise level of the system depends on the external input capacitance. If exceptionally long cables are used, or low measuring thresholds employed, then the charge sensitive amplifier must be a low noise type.

Current amplification

An open output multiplier with separate collector electrode should be used for current measurements. The collector electrode is biased positively, as shown in Fig. 10, to ensure collection of all output electrons. Care must be taken to prevent ionic feedback round the outside of the device.

For satisfactory linearity the multiplier should be operated with a gain of less than 10^5 and the output current should not exceed 1% of the standing current. The multiplier should be calibrated at intervals because the gain changes during life and is a very sensitive function of voltage at low values. From Fig. 2 it can be seen that a small change in voltage produces a large change in gain.

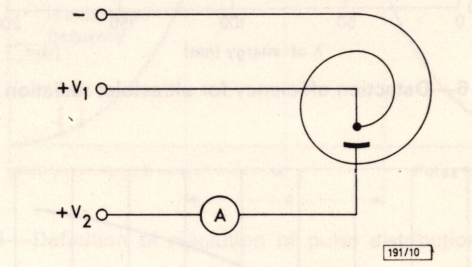

Fig. 10—Basic current measuring circuit

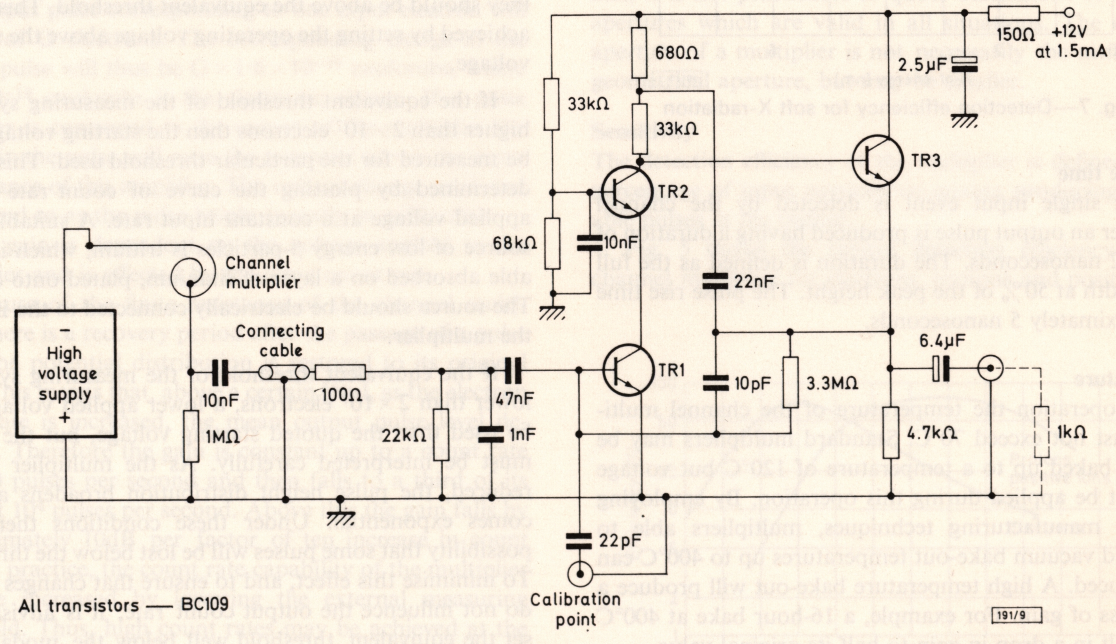

Fig. 9—Channel multiplier with charge sensitive amplifier

If the channel multiplier gain = 10^8 and the output pulse = 0·5V+ve, then the output pulse width ≈ 20μs, the maximum count rate ≈ 10^4 pulse/sec and the noise level ≈ 0·005V

Reliability and stability of carbon film resistors

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UDC 621.316.849: 620.169

Performance in life, climatic, noise and other tests is evaluated and details of the tests are given. The reliability was found to be $0{\cdot}10\times10^{-6}$ *failures per hour for values under 1MΩ or* $0{\cdot}9\times10^{-6}$ *failures per hour for values above 1MΩ. Failure rate in field tests was* $0{\cdot}052\times10^{-9}$ *failures per hour.*

INTRODUCTION

Carbon film resistors in two physical sizes have been marketed by Mullard for many years; and a third and larger size has now been added to the range. In 1967 the system of rating these resistors was drastically changed, the old wattage rating being discontinued and replaced by a nomogram relating power dissipation and ambient temperature to life stability. (Ref. 1).

Resistors are perhaps the most widely used of all electronic components, therefore there is a need for complete information about their behaviour.

This article gives information on the performance of these resistors under laboratory test conditions; under conditions of field usage; and in terms of internationally accepted specifications.

CONSTRUCTION

The method of construction of all styles of carbon film resistor is similar. By pyrolysis of a hydrocarbon gas, a hard homogeneous film of carbon is deposited on to a high grade ceramic rod. Contact caps of a special alloy are then pressed on to the ends of the resistor body and tinned electrolytic copper leads welded to these caps. The required resistance value cannot usually be obtained by pyrolysis alone. A helical groove is cut through the carbon film, and the finer the pitch of the helix the higher the resistance value. Finally, the resistors are coated with several coats of lacquer for electrical, mechanical and climatic protection.

An outline drawing and dimensions are given in Fig. 1. The three styles of resistor are differentiated by their physical size rather than by their power rating. Electrical properties are summarised in Table 2.

The limiting voltage (element and insulation) is the maximum permissible voltage that may be applied continuously to the resistor element (see IEC publication 115, clause 1.3.5.). It is also the maximum voltage that may be applied continuously to the insulation of the resistor.

RELIABILITY AND STABILITY

The first part of this article presents the results of many tests and investigations carried out by the Quality and Reliability Laboratories of the company in close cooperation with development groups and production divisions over a period of five years. It discusses performance changes observed in that period; in particular, an assessment of failure rate and life stability is made.

Various definitions of failure may be used. For example, resistors which drift outside their tolerance or drift by 1, 2, or 3% of their nominal value under specified test conditions may be classified as failures. These changes in performance of the component are not necessarily related

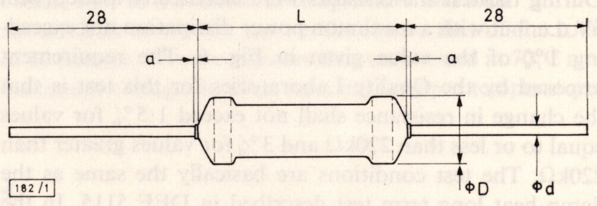

Fig. 1—Outline of Mullard carbon film resistors

TABLE 1

Dimensions of the various styles in mm

	D_{max}	L_{max}	a_{max}	d
CR16	1·6	4·5	1·0	0·4
CR25	2·5	7·5	1·0	0·6
CR37	3·7	10	1·0	0·7

TABLE 2

Range of electrical properties

	Resistance range min	Resistance range max	Series	Tolerance (± %)	Limiting voltage (V r.m.s.)
CR16	10Ω	220kΩ	E12	5	150
	270kΩ	1MΩ		10	150
CR25	1Ω	1MΩ	E12	5	250
	1·2MΩ	10MΩ		10	250
CR37	1Ω	1MΩ	E24	5	350
	1·2MΩ	10MΩ	E12	10	350

This article is based on work done by P. Popkema, Quality and Reliability Laboratory, Elcoma Division, Philips, Eindhoven.

1) STANLEY, K. W. 'Ratings of carbon film resistors' Mullard Technical Communications, Vol. 9, No. 86, pp 144 to 148.

to the malfunction of the equipment in which they are used. In the Mullard system, drift in value is considered as a stability problem and a nomogram is produced relating these changes with life under various combinations of load and ambient temperature. Reliability information is presented in the form of observed failure rates based on the total number of failures in a single population and the total observed time of that population. Under this heading only catastrophic failures are included.

It is considered that this separation of reliability and stability gives the equipment designer more information enabling him to assess the performance of the resistor accurately under his own working conditions.

TESTS AND MEASUREMENTS

The resistors investigated were random samples taken regularly from production over the period 1965 to 1970. The sampling was such that the results are representative of the entire production during that period. The main tests carried out included life, damp heat, and temperature rapid change followed by damp heat.

Life tests were performed at various combinations of temperature and loading (intermittent 1·5 hours on and 0·5 hour off) the maximum test duration being 10 000 hours.

Damp heat tests (long term exposure) were carried out in accordance with IEC publication 68-2 Test C consisting of 56 days at 40°C and relative humidity of 90 to 95%. During the test the resistors were electrically loaded with 5V d.c. but with a maximum power dissipation not exceeding 1% of the value given in Fig. 6. The requirement imposed by the Quality Laboratories for this test is that the change in resistance shall not exceed 1·5% for values equal to or less than 220kΩ and 3% for values greater than 220kΩ. The test conditions are basically the same as the damp heat long term test described in DEF 5115. In the DEF specification, however, the resistors are loaded with 0·2% of their rated power at 70°C subject to a minimum applied voltage of 1·0V. The maximum permissible change of resistance for carbon film resistors according to DEF 5115-1 Style RFG3 is 2% for all values.

Rapid change of temperature tests were carried out in accordance with IEC 68-2 Test Na in which the conditions are 3 hours at −55°C followed by 3 hours at +155°C, this cycle being performed five times. Test requirements are that the resistance shall not change by more than 0·5% or 0·5Ω, whichever is the greater.

In a further test sequence this was immediately followed by a damp heat test to IEC 68-2 Test C under the conditions previously given except that during this test the resistors were not loaded.

The corresponding test in the DEF specifications is the temperature rapid change in which the conditions are 1 hour at −55°C followed by 1 hour at +125°C, this cycle being repeated ten times in total. The test requirement is a maximum resistance change of 0·2%. In the DEF specification the temperature rapid change test is followed by a climatic sequence consisting of dry heat, dry cold, damp heat accelerated and low air density cycles. It cannot be compared directly with the test carried out above, namely the temperature rapid change followed by the long term damp heat.

RELIABILITY

In this section only catastrophic failures, that is complete interruptions, are taken into account. The stability of the resistors or their resistance to change in their properties is dealt with in a later section.

The failure rate is given as failures per hour with a confidence level of 60%. To obtain this confidence level the number of failures actually recorded is artificially raised by adding a constant C60 based on the Poisson distribution and the failure rate is calculated as

$$\text{F.R. } (60\%) = \frac{\text{number of recorded failures } + \text{C60}}{\text{number of component test hours}}.$$

The failure rate thus calculated is an average for all values from the relevant production period and is valid for the conditions in which the tests were carried out. The failure rates are further analysed, and the dependence on design, value, test duration, temperature, load, etc. is examined in more detail in subsequent sections.

Failure rate in long life test

A large number of resistors of different values and styles are regularly subjected to long term life tests with a maximum duration of 10 000 hours. These tests are carried out at different resistor body hot-spot temperatures ranging from 25°C to the maximum of 155°C. These hot-spot temperatures are obtained from various combinations of ambient temperature and load and are so chosen that the different styles and values are tested at about the same hot-spot temperatures.

Fig. 2 gives a survey of the test programme, the chosen conditions being indicated by dots, each dot representing several styles and values.

Table 3 is a survey of the life test results. Since analysis of the results showed that there is a relationship between failure rate and resistance value the results for the values less than 1MΩ and greater than 1MΩ are shown separately.

TABLE 3

Assessed failure rates of carbon film resistors in life tests at various hot-spot temperatures (25°C to 155°C, see Fig. 2)

	number tested	unit hours	failures
Nominal value ≤1MΩ			
CR16	9528	24 096 376	2
CR25	7432	37 201 408	6
CR37	12 563	50 651 648	3
Total	29 523	111 949 432	11
Failure rate 60% confidence	0·11 × 10⁻⁶/hour		
Nominal value > 1MΩ			
CR16	406*	437 896	0
CR25	3016	8 818 240	11
CR37	4398	10 052 216	4
Total	7820	19 308 352	15
Failure rate 60% confidence	0·80 × 10⁻⁶/hour		

*Since early 1968 the resistance values >1MΩ of the CR16 have not been available.

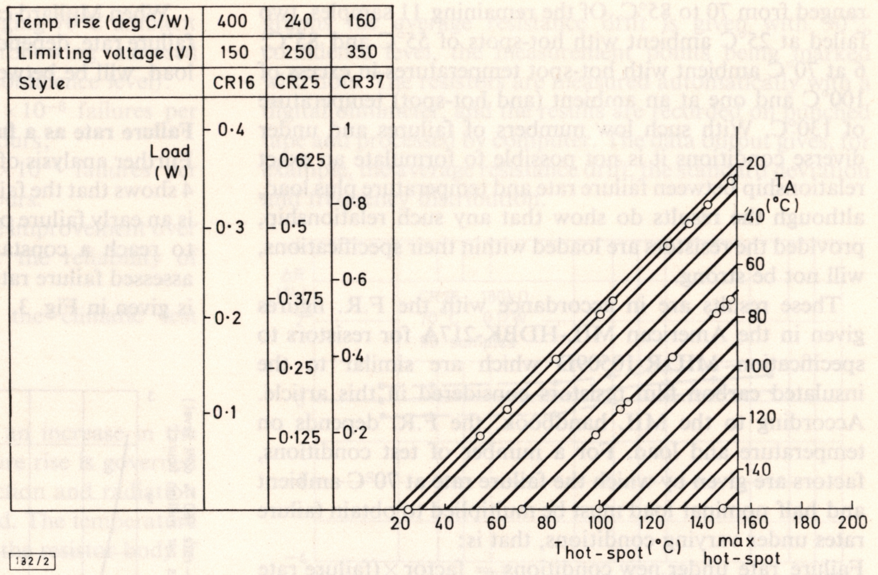

Fig. 2—Testing diagram for carbon film resistors

The results given in Table 3 concern life tests performed under various conditions, and the assessed failure rates are average values valid for the test conditions given in Fig. 2 and a total test duration of 10 000 hours. The relationship between failure rate and temperature will be further discussed in the next section. Table 3 gives a very favourable failure rate for values less than 1MΩ, and for the higher values the failure rate remains satisfactory.

The results show that there is no significant difference between the various styles, accordingly one F.R. is quoted for the complete range.

Table 4 details all the failures that occurred during these tests.

Failure rate as a function of temperature and load

An analysis of the life test results shows that of the total of 26 failures, 17 were resistors that were tested at 70°C and maximum voltage. In these tests the hot-spot temperatures

TABLE 4

Specification of failures

	Nominal value	Number of failures	Failure time (hrs)	Test conditions			Hot-spot in test (°C)	Limiting voltage (V d.c.)
				Temp. (°C)	Load (W)	(V)		
CR16	180kΩ	1	1000	70	0·1	134	110	150
CR16	680kΩ	1	1000	70	max V	150	83	150
CR25	47Ω	1	4032	130	no load	—	130	250
CR25	180kΩ	1	24	25	0·25	210	85	250
CR25	180kΩ	1	24	70	0·25	210	130	250
CR25	220kΩ	1	24	70	0·25	230	130	250
CR25	470kΩ	1	24	25	0·15	242	55	250
CR25	1MΩ	1	1008	70	max V	250	84	250
CR25	1·2MΩ	1	48	70	max V	250	75	250
CR25	3·9MΩ	1	168	70	max V	250	72	250
CR25	4·7MΩ	1	1008	70	max V	250	71	250
CR25	10MΩ	2	1008	70	max V	250	71	250
CR25	10MΩ	1	168	70	max V	250	71	250
CR25	10MΩ	5	504	70	max V	250	71	250
CR37	220kΩ	1	24	70	0·25	237	110	350
CR37	220kΩ	1	24	70	0·50	332	150	350
CR37	470kΩ	1	4032	70	0·25	340	110	350
CR37	3·3MΩ	1	216	70	max V	350	75	350
CR37	6·8MΩ	1	24	70	max V	350	72	350
CR37	6·8MΩ	1	96	70	max V	350	72	350
CR37	10MΩ	1	1000	70	max V	350	72	350

ranged from 70 to 85°C. Of the remaining 11 samples, two failed at 25°C ambient with hot-spots of 55°C and 85°C; 6 at 70°C ambient with hot-spot temperatures in excess of 100°C and one at an ambient (and hot-spot) temperature of 130°C. With such low numbers of failures and under diverse conditions it is not possible to formulate an exact relationship between failure rate and temperature plus load, although the results do show that any such relationship, provided the resistors are loaded within their specifications, will not be strong.

These results are in accordance with the F.R. figures given in the American MIL-HDBK-217A for resistors to specification MIL-R-10509D which are similar to the insulated carbon film resistors considered in this article. According to the MIL handbook, the F.R. depends on temperature and load. For a number of test conditions, factors are given by which the failure rate at 70°C ambient and half nominal load must be multiplied to obtain failure rates under varying conditions, that is:

Failure rate under new conditions = factor × (failure rate at 70°C, half load).

TABLE 5

Failure rate factors as a function of temperature and load in accordance with MIL-HDBK-217A for type MIL-R-10509D

Conditions		Factor
Amb. temp. (°C)	**Load**	
25	0·1 nom	0·38
25	0·5 nom	0·56
25	nom	1·05
70	0·1 nom	0·64
70	0·5 nom	1·0
70	nom	2·27
125	0·1 nom	1·36
125	0·5 nom	2·27

The failure rates for Mullard carbon film resistors given in the previous section were calculated from all the life test results obtained and are therefore average values. They can therefore be regarded as the failure rate at 70°C ambient with half nominal load yielding a hot-spot temperature of approximately 110°C. The factors given in Table 5 can be used to estimate the failure rate under other conditions of use.

The extreme conditions are 25°C ambient with 0·1 nominal load giving a hot-spot of about 30°C, and, at the other extreme, 125°C ambient with 0·5 nominal load giving a hot-spot of 155°C.

The corresponding failure rates calculated from Table 3 and the factor given above are shown in Table 6.

TABLE 6

Failure rates as a function of temperature and load

Conditions		Hot-spot	Failure rate per hour at 60% confidence level	
Amb. temp. (°C)	**Load**	**temperature (°C)**	**R_{nom} $\leqslant 1M\Omega$**	**R_{nom} $>1M\Omega$**
25	0·1 nom	30	$0{\cdot}042\times10^{-6}$	$0{\cdot}30\times10^{-6}$
125	0·5 nom	155	$0{\cdot}25\times10^{-6}$	$1{\cdot}8\times10^{-6}$

When Mullard carbon film resistors are used the assessed failure rate, depending upon conditions of temperature and load, will be between the limits of Table 6.

Failure rate as a function of test duration

Further analysis of the failure figures given in Tables 3 and 4 shows that the failure rate is not constant with time. There is an early failure period during which the failure rate drops to reach a constant value after about 2000 hours. The assessed failure rate for both values above and below 1MΩ is given in Fig. 3.

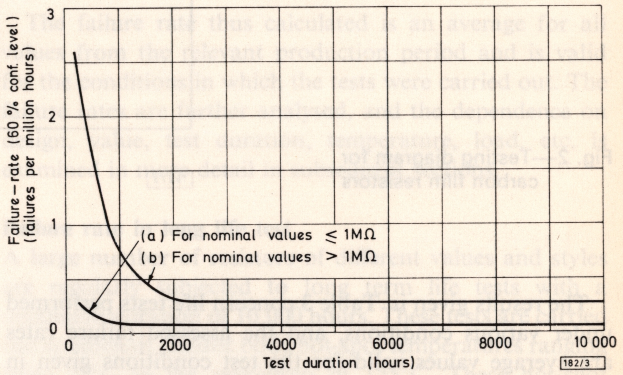

Fig. 3—Assessed failure rate as a function of the life test duration at various hot-spot temperatures

If failures occurring before the completion of the first thousand hours of the test are eliminated from the results given in Tables 3 and 4, the failure rates for values below and above 1MΩ are $0{\cdot}07\times10^{-6}$/hour and $0{\cdot}35\times10^{-6}$/hour respectively.

Reliability in climatic tests

The failure data in climatic tests provide supplementary information where the climatic conditions are appropriate.

The samples were divided into two approximately equal lots. The first lot underwent a damp heat test at 40°C and 90 to 95% R.H. lasting 56 days. The resistors were at a potential of 5Vd.c. or a power dissipation 1% of the value indicated by Fig. 6, whichever was the least. The remaining samples underwent a temperature cycling test followed by a damp heat test. The resistors were at a temperature of 155°C for three hours and −55°C for three hours. This cycle was repeated five times immediately after which they were tested at 40°C and 90 to 95% R.H. at no load for 56 days.

A total of 977 resistors were tested and no failures were found. The estimated failure rate with a 60% confidence level is less than 0·09% per thousand hours.

Reliability conclusions

1) The failure rate as a function of time is not constant, a higher rate occurring during the first 2000 hours.
2) No significant difference in F.R. was observed between the three styles, CR16, CR25 and CR37.
3) Temperature and load have little effect provided that the resistors are loaded within their rating.
4) Under the test conditions averaging 70°C ambient and half nominal load the following assessed failure rates were found (60% confidence level):
   Resistance values ≤1MΩ $0{\cdot}10\times10^{-6}$ failures per hour or 0·01% per thousand hours;
   Resistance values >1MΩ $0{\cdot}9\times10^{-6}$ failures per hour or 0·09% per thousand hours.
   These results show a considerable improvement over previously accepted figures for the reliability of carbon film resistors.
5) No failures occurred during the climatic test sequence.

STABILITY

Power dissipation in a resistor causes an increase in the temperature of its body. The temperature rise is governed by the laws of heat conduction, convection and radiation and is proportional to the electrical load. The temperature will show a maximum in the middle of the resistor body if it is of symmetrical construction.

The temperature rise in degrees C is

$$\Delta T = A.P,$$

where A is the temperature rise in degrees C per watt load (the heat resistance) and P is the load in watts.

The heat resistance is dependent on the dimensions of the resistor, the heat conductivity of the materials used, and to a lesser extent the method of mounting.

The sum of the temperature rise ΔT and the ambient temperature T_A is the maximum or hot-spot temperature T_M of the resistor.

$$T_M = T_A + \Delta T = T_A + A.P.$$

therefore

$$P = (T_M - T_A)/A.$$

If P is plotted against T_M, for a constant value of A, parallel straight lines are obtained for different values of the ambient temperature. The slope of these lines $dP/dT_M = 1/A$ is the reciprocal of the heat resistance and is characteristic for a given size and construction of resistor.

The stability of a carbon film resistor is determined primarily by the hot-spot temperature and the resistance value. For the first approximation of the stability it is therefore immaterial how (temperature and load combined) the hot-spot temperature is obtained. The influence of the resistance value originates from the greater film thickness of the lower resistance values. The stability expressed as $\Delta R/R$ can be determined experimentally, for instance after 1000 hours as a function of the hot-spot temperature with resistance value as a parameter. It has been found that resistance changes exponentially with time, giving a straight line when log $\Delta R/R$ is plotted against T_M. A combination of two graphs, P against T_M and $\Delta R/R$ against T_M, gives a nomogram from which the values of stability can be ascertained for power dissipation and ambient temperature.

Resistors to be tested in accordance with the diagram in Fig. 2 are measured at set times during the test and the results plotted. In Fig. 4 the resistance drift of different styles and values has been plotted against test duration for different combinations of temperature and load. In these graphs the average resistance drift is given with 90% confidence level, the measurement points being marked with dots. The resistors are measured automatically with a digital ohmmeter, and the results are recorded on punched tape and processed by computer. The data output gives, for example, the average resistance drift, the standard deviation and frequency distribution.

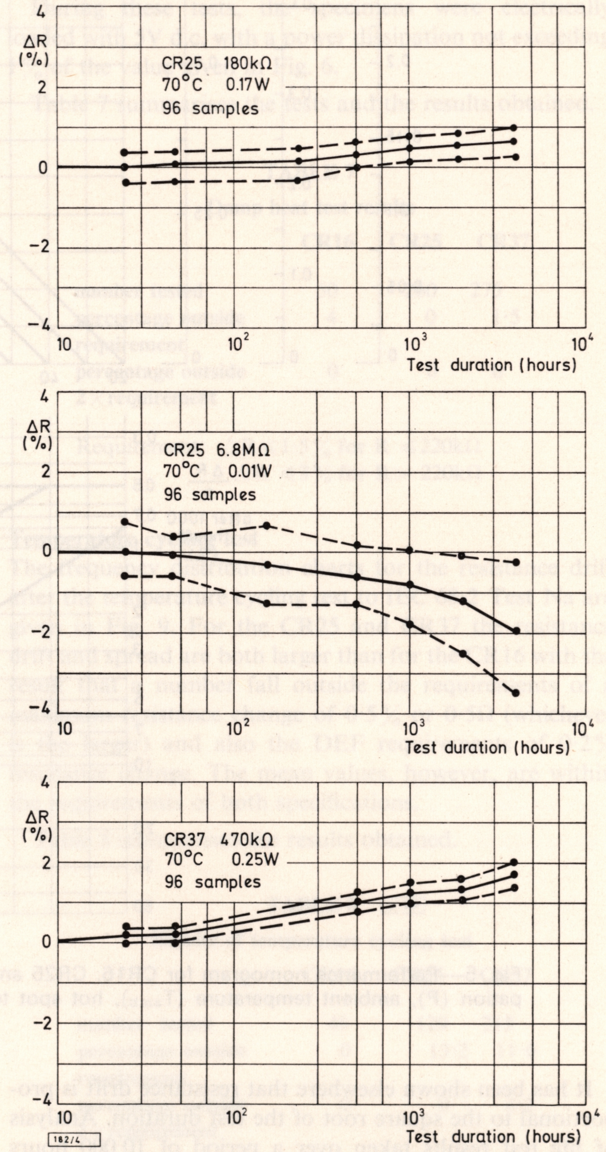

Fig. 4—Resistance drift (ΔR) as a function of the test duration under different conditions and for three different values

——— – – – average and 90% confidence limits

All the results, plotted as the examples shown in Fig. 4, were further analysed and used to construct the nomogram of Fig. 5. The 95% confidence limits for resistance drift after a test duration of 1000 hours for various nominal resistance values are given in the bottom corner of the figure. The upper half of the nomogram indicates the hot-spot temperature corresponding to a certain load and ambient temperature. The hot-spot temperature is plotted along the horizontal axis.

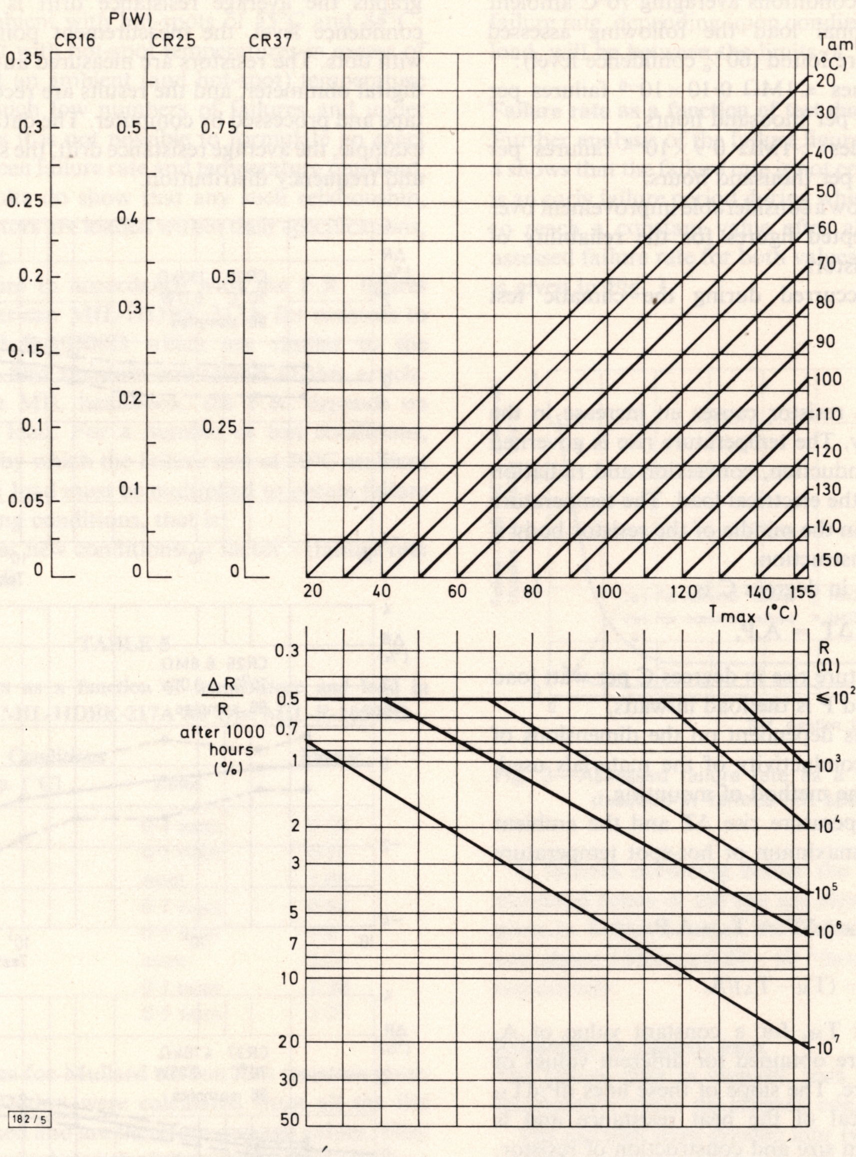

Fig. 5—Performance nomogram for CR16, CR25 and CR37, showing the relationship between power dissipation (P), ambient temperature (T_{amb}), hot spot temperature (T_{max}) and stability ($\Delta R/R$) for 1000 hours

It has been shown elsewhere that resistance drift is proportional to the square root of the test duration. Analysis of life test results taken over a period of 10 000 hours shows that Mullard carbon film resistors follow this pattern.

In practical cases the nomogram may be used to determine (a) the drift occurring in a specific resistor operating under known conditions or (b) the style of resistor which must be used to fulfil specified drift conditions. When using the nomogram neither the maximum hot-spot temperature of 155°C nor the limiting voltage rating specified in Table 1 should be exceeded.

IEC publication 115 'Recommendations for Fixed Non-wirewound Resistors Type 1' and the British Defence Specification DEF 5115-1 'Detail Specification for Resistors, Fixed, General Purpose', are both based on the conventional method of rating resistors by a fixed 'rated dissipation' at 70°C with an associated load life stability. In the Mullard rating system, the rated dissipation is no longer specified. Instead, a guaranteed stability (to a 95% confidence level) has been made a function of the operating conditions.

Fig. 6 shows the maximum power dissipation of the three Mullard styles CR16, CR25 and CR37 under the IEC test conditions: namely the maximum permissible dissipation in a 70°C ambient for a resistance drift of 1·5% max for all resistance values, a hot-spot temperature of 155°C and limiting voltage as in Table 1.

Fig. 7 is a similar graph constructed for the test conditions imposed by the DEF 5115-1 specification Style RFG3: namely the maximum dissipation at 70°C for a resistance drift of 2·0% maximum after 2000 hours of test, a limiting hot-spot temperature of 150°C and limiting voltage as Table 1.

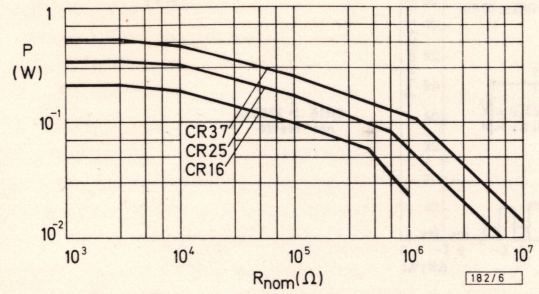

Fig. 6—Maximum permissible dissipation at an ambient temperature of 70°C as a function of the resistance value under the conditions specified in IEC 115. Maximum hot-spot temperature: 155°C, the limiting voltage taken into account. Maximum resistance drift: 1·5% for nominal values ≤ 220kΩ, and 3% for nominal values > 220kΩ after 1000 hours

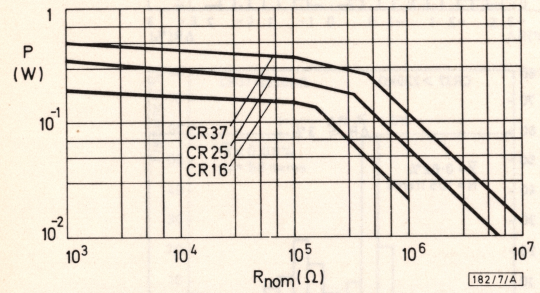

Fig. 7—Maximum permissible dissipation at an ambient of 70°C as a function of the resistance value in accordance with DEF 5115 Style RFG3. Hot-spot temperature 150°C maximum, the limiting voltage taken into account. Maximum resistance drift of 2·0% after 2000 hours

The conclusions drawn from the life tests are:

1) Stability depends upon the hot-spot temperature and nominal resistance value.
2) A 10 degC increase in hot-spot temperature causes resistance drift $\Delta R/R$% to increase by a factor of 1·25 for 1MΩ resistors to about 1·4 for 1kΩ resistors.
3) During life, the resistance drift is proportional to the square root of time.

Stability in climatic tests
The frequency distributions of the resistance drift during the climatic tests are given in Fig. 8. Two distributions are given per style, one for nominal values ≤220kΩ and one for values >220 kΩ.

The results of the temperature cycling test are given in Fig. 9. Only one distribution is given here since analysis of the results showed no significant differences between low and high nominal values.

Damp heat test
The frequency distribution of the resistance drift ($\Delta R/R$) in the long term damp heat test (to IEC 68-2 Test C) are given in Fig. 8. These graphs show that the drift and the spread are greatest for the higher resistance values. Practically all samples meet our requirements. The DEF specification imposes a resistance drift of 2% max on all resistance values after a similar 56-day long-term damp heat test. The graphs show that practically all samples meet these requirements.

During these tests, the specimens were electrically loaded with 5V d.c. with a power dissipation not exceeding 1% of the value given in Fig. 6.

Table 7 summarises the tests and the results obtained.

TABLE 7

Damp heat test results

	CR16	**CR25**	**CR37**
number tested	50	260	275
percentage outside requirement	4	0	1·5
percentage outside 2×requirement	0	0	0

Requirement: ΔR ≤ 1·5% for R ≤ 220kΩ
ΔR ≤ 3% for R > 220kΩ

Temperature cycling test
The frequency distribution charts for the resistance drift after the temperature cycling test to IEC 68-2 Test Na are given in Fig. 9. For the CR25 and CR37 the resistance drift and spread are both larger than for the CR16 with the result that a number fall outside the requirements of a maximum resistance change of 0·5% or 0·5Ω (whichever is the larger) and also the DEF requirements of 0·2% resistance change. The mean values, however, are within the requirements of both specifications.

Table 8 summarises the results obtained.

TABLE 8

Results of temperature cycling test

	CR16	**CR25**	**CR37**
number tested	48	129	215
percentage outside requirement	0	13·2	11·6
percentage outside 2×requirement	0	0	4·2

Requirement: ΔR ≤ 0·5% or 0·5Ω

Temperature cycling followed by damp heat test
Further samples were subjected to the temperature cycling test described above and immediately followed by the 56-day damp heat test. The specimens were not loaded. The results are shown in Fig. 10 and summarised in Table 9. Again the higher resistance values show the greater change and spread in properties after this combined test.

The tests are in accordance with the IEC specification. There is no directly comparable test in the DEF specification. In this the temperature cycling test is followed by a climatic test sequence.

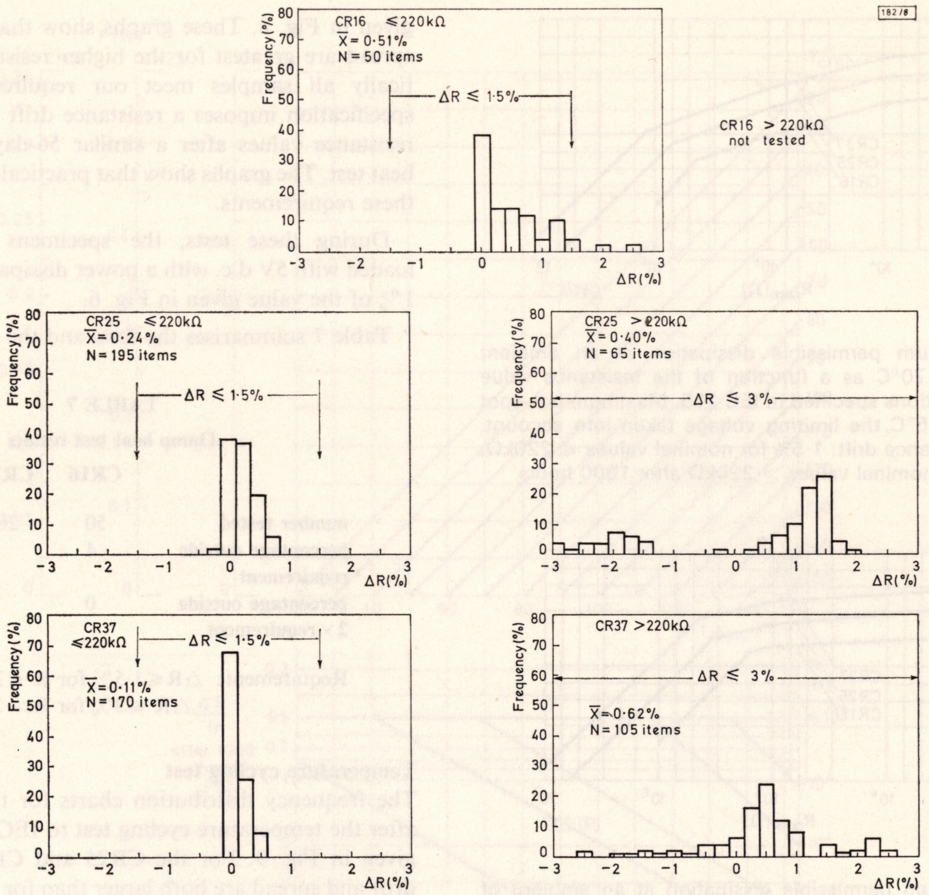

Fig. 8—Frequency distributions of resistance drift in damp heat long term test

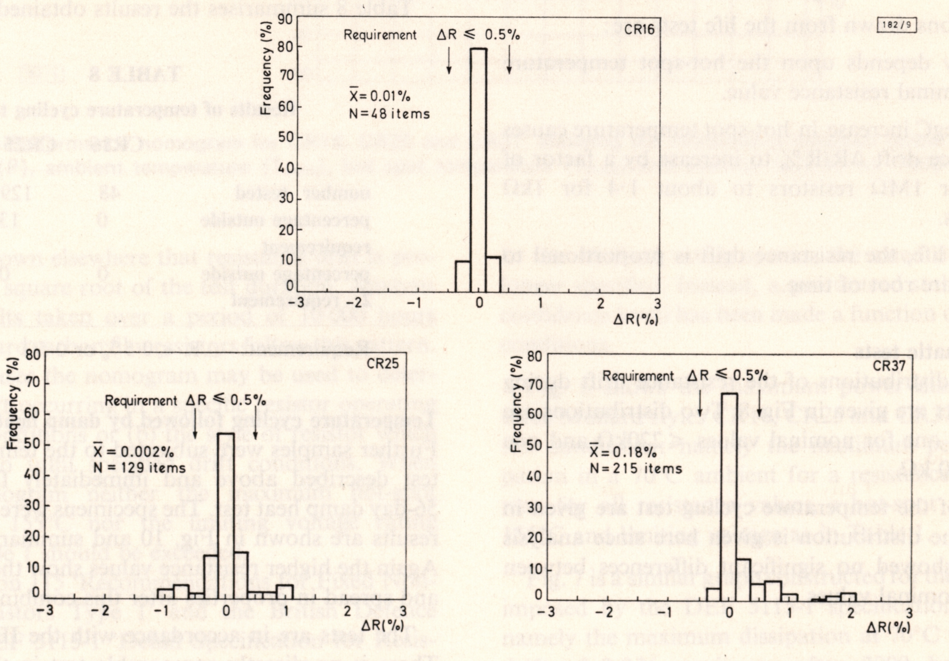

Fig. 9—Frequency distributions of resistance drift in temperature cycling test

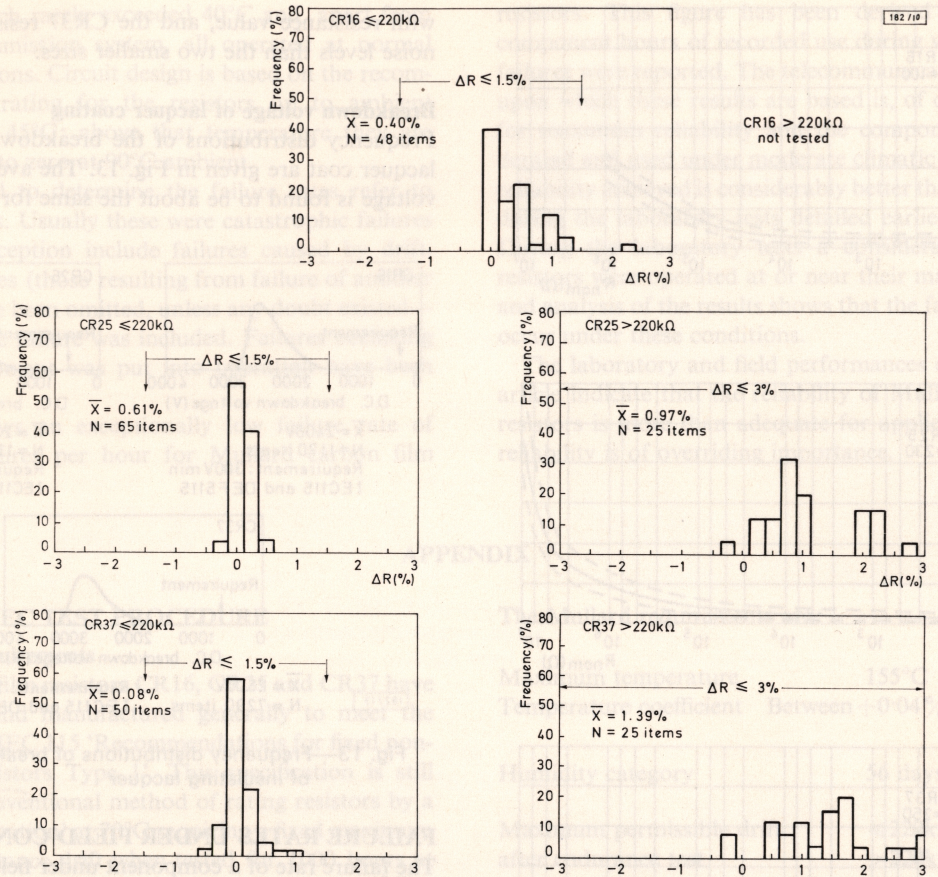

Fig. 10—Frequency distributions of resistance drift in the temperature cycling test followed by damp heat long term test

TABLE 9

Temperature cycling followed by damp heat test results

	CR16	CR25	CR37
number tested	48	90	75
percentage outside requirement	2	0	0
percentage outside 2 × requirement	0	0	0

Requirement: $\Delta R \leqslant 1{\cdot}5\%$ for $R \leqslant 220\mathrm{k\Omega}$
$\Delta R \leqslant 3\%$ for $R > 220\mathrm{k\Omega}$

Additional measurements

In addition to the measurements described in the preceding sections, the quality control system continually monitors other characteristics of the resistors. These measurements make it possible to detect any deterioration in a characteristic with time although specification limits are maintained. The actual level of these characteristics is summarised in the following sections.

Temperature coefficient

The temperature coefficient of resistance is measured between 30°C and 80°C. In Fig. 11, the temperature coefficient is plotted as a function of the nominal resistance. The graph is applicable to all styles since analysis of the results showed no significant differences in temperature coefficient between them.

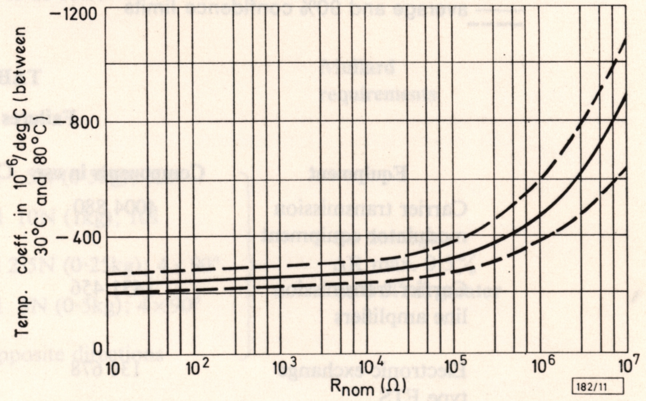

Fig. 11—Temperature coefficient as a function of resistance value (all styles)

average and 90% confidence limits, N = 485 items

Noise

Noise measurements are carried out with a Resistor Noise Test Set model 315 manufactured by Quan Tech Laboratories. The three graphs of Fig. 12 show noise as a function of nominal resistance for different styles. Noise increases

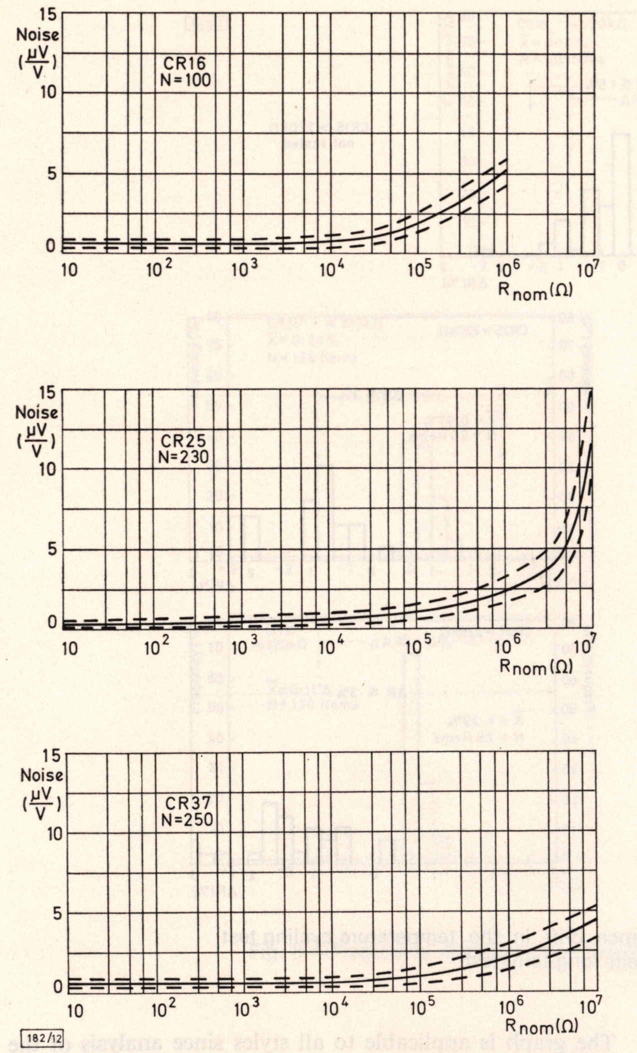

Fig. 12—Noise as a function of nominal resistance value

average and 90% confidence limits

with resistance value, and the CR37 resistors have lower noise levels than the two smaller sizes.

Breakdown voltage of lacquer coating

Frequency distributions of the breakdown voltage of the lacquer coat are given in Fig. 13. The average breakdown voltage is found to be about the same for the three styles.

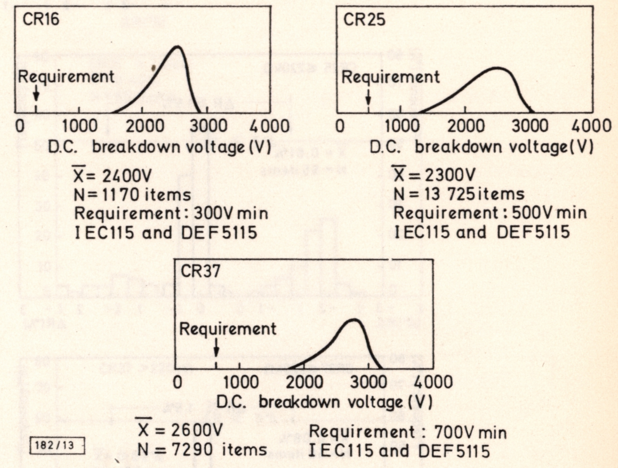

Fig. 13—Frequency distributions of breakdown voltage of insulating lacquer

FAILURE RATES UNDER FIELD CONDITIONS

The failure rate of a component under field conditions can be estimated only if complete details of operating time and failures are available. Table 10 shows results obtained from a carrier transmission system in operation between 1962 and 1969, electronic telephone exchanges in operation between 1966 and 1969, and processors for telegraphy systems.

The components used in the carrier transmission system were in sealed units ensuring a relative humidity of less than 25%. All equipments operated at a fairly stable temperature which rarely exceeded 40°C and, apart from the carrier transmission system, all operated at normal humidity conditions. Circuit design is based on the recommended power rating for the resistors up to ambient temperatures of 45°C; above that temperature they are derated linearly to zero at 90°C ambient.

The data used to determine the failure rates refer to complete failures. Usually these were catastrophic failures and only by exception include failures caused by drift. Secondary failures (those resulting from failure of another component) have been omitted, unless any doubt existed—in which case the failure was included. Failures occurring before the equipment was put into operation have been left out.

TABLE 10

Failures in the field

Equipment	Components in use	Component hours	Failures	Failure rate*
Carrier transmission modulator equipment	4004 880	89 620 × 10^6	3	0·075 × 10^{-9}
Carrier transmission line amplifiers	1431 456	32 726 × 10^6	0	0·071 × 10^{-9}
Electronic exchange type ETS	131 678	1899 × 10^6	0	1·2 × 10^{-9}
Electronic exchange type UV	64 845	573 × 10^6	0	4·0 × 10^{-9}
Telegraphy processor	340 244	5279 × 10^6	0	0·45 × 10^{-9}
	5973 103	130 097 × 10^6	3	0·052 × 10^{-9}

*Note: The failure rate is in units per hour at a 90% confidence level. In earlier sections of this article a 60% confidence level has been used.

Table 10 shows an exceptionally low failure rate of 0·052 × 10^{-9} failures per hour for Mullard carbon film resistors. This figure has been derived after 130 × 10^9 component hours of recorded use during which only three failures were reported. The telecommunications equipment upon which these results are based is, of course, designed for maximum reliability and the components have been derated and used under moderate climatic conditions. The reliability achieved is considerably better than that obtained during the laboratory tests detailed earlier in this article. During the laboratory tests a considerable number of resistors were operated at or near their maximum ratings, and analysis of the results shows that the failures tended to occur under these conditions.

The laboratory and field performances discussed in this article indicate that the reliability of Mullard carbon film resistors is more than adequate for applications in which reliability is of overriding importance.

APPENDIX

IEC TEST PROCEDURE

Specification requirements

Mullard carbon film resistors CR16, CR25 and CR37 have been designed and manufactured generally to meet the requirements of IEC 115 'Recommendations for fixed non-wire wound resistors Type 1'. This specification is still based on the conventional method of rating resistors by a fixed 'rated dissipation' at 70°C requiring a fixed maximum permissible resistance drift when tested for 1000 hours at the rated dissipation. With the Mullard system a rated dissipation is no longer given but use is made of a nomogram to link dissipation, ambient temperature and stability.

The Mullard requirements are:

Maximum temperature	155°C
Temperature coefficient	Between +0·04%/degC and −0·10%/degC
Humidity category	56 days
Maximum permissible drift after endurance test	≤220kΩ ≤1·5% >220kΩ ≤3%
Maximum permissible drift after damp heat long term test	≤220kΩ ≤1·5% >220kΩ ≤3%

For the testing programme the samples are divided into four lots. The test programme is as follows:

LOT ONE

IEC 115 clause	IEC 68 test method	Test	Procedure	Mullard requirements
2.5.1		Robustness of terminations		
	Ua	a. Tensile all samples	0·4mm: load 5N (0·5kg); 10s 0·6mm, 0·7mm load 10N (1kg); 10s	no damage ΔR max. 0·5% or 0·5Ω if greater
	Ub	b. Bending half number of samples	0·4mm: load 2·5N (0·25kg); 4×90° 0·6mm, 0·7mm load 5N (0·5kg); 4×90°	
	Uc	c. Torsion other half number of samples	2×360° in opposite directions	
2.5.2.	T2	Soldering (globule method)	solderability: 2s 230°C 0·5% activated flux thermal shock: 3s 350°C, 6mm from body	good tinning, no damage ΔR max. 0·5% or 0·5Ω if greater
—	Na	Rapid change of temperature	3 hours −55°C/3 hours 155°C 5 cycles	ΔR max. 0·5% or 0·5Ω if greater

IEC 115 clause	IEC 68 test method	Test	Procedure	Mullard requirements
2.5.3.	FB IV	Vibration	Frequency: 10 to 500Hz: displacement 1·5mm or acceleration 10g: three directions: total 9h	no damage ΔR max. 0·5% or 0·5Ω if greater
—	—	Bumping	3×1500 bumps in three directions: 50g	no damage ΔR max. 0·5% or 0·5Ω if greater
		Climatic sequence		
2.6.1.	B II	Dry heat	16 hours 155°C	
2.6.2.	D IV	Damp heat (accel) 1st cycle	1 day: 55°C: 95 to 100% R.H.	
2.6.3.	A IV	Cold	2 hours: −55°C	
2.6.4.	M IV	Low air pressure	1 hour: 85 mbar: 15 to 35°C	
2.6.5.	D IV	Damp heat (accel) remaining cycles	5 days: 55°C: 95 to 100% R.H.	R_{ins}: min. 1000MΩ ΔR max. 1·5% for R⩽220kΩ 3% for R>220kΩ
2.6.6.2.	—	Load	24 hours: room temp: load taken from Fig. 6	ΔR max. 1·5% for R⩽220kΩ 3% for R>220kΩ
LOT TWO				
2.7	C IV	Damp heat (long term exposure)	56 days: 40°C: 90 to 95% R.H. 5V d.c. on half the number of specimens, but the dissipation should not exceed 1% of the value indicated by Fig. 6.	R_{ins}: min. 1000MΩ ΔR max: 1·5% forR⩽220kΩ max: 3 %for R>220kΩ
2.7.5.	—	Load	24 hours: room temp: dissipation taken from Fig. 6.	ΔR as above
LOT THREE				
2.9.	—	Endurance	1000 hours: 70°C: dissipation taken from Fig. 6	ΔR max.: 1·5% for R⩽220kΩ 3% for R>220kΩ
LOT FOUR				
2.4.2.	—	Insulation resistance		min. 10^4 MΩ
2.4.3.	—	Temperature coefficient	between −55°C and +155°C	+0·004%/degC to −0·1%/degC
2.4.5.	—	Voltage proof on insulation	2×limiting voltage, a.c., 1 min.	No breakdown
2.4.6.	—	Noise	IEC publication 195	
—	—	Short time overload	room temperature, dissipation 6·25×value taken from Fig. 6 (voltage not more than 2×limiting voltage) 10 cycles, 4 seconds on, 45 seconds, off	ΔR max. 1%
—	—	Voltage coefficient	—	<5 p.p.m.

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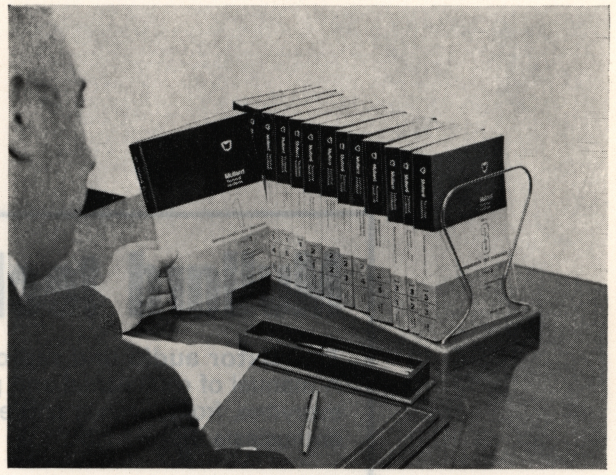

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